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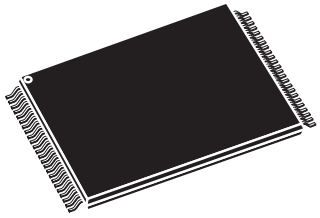
NAND04GW3B2B
NAND08GW3B2A

4 Gbit, 8 Gbit, 2112 Byte/1056 Word Page 3V, NAND Flash Memories

PRELIMINARY DATA

Feature summary

- High density NAND Flash Memory
  - up to 8 Gbit memory array
  - Up to 256 Mbit spare area
  - Cost effective solution for mass storage applications
- NAND Interface
  - x8 bus width
  - Multiplexed Address/ Data
- Supply voltage
  - 3.0V device: V_{DD} = 2.7 to 3.6V
- Page size
  - (2048 + 64 spare) Bytes
- Block size
  - (128K + 4K spare) Bytes
- Page Read/Program
  - Random access: 25µs (max)
  - Sequential access: 30ns (min)
  - Page program time: 200µs (typ)
- Copy Back Program mode
  - Fast page copy without external buffering
- Cache Program and Cache Read modes
  - Internal Cache Register to improve the program and read throughputs
- Fast Block Erase
  - Block erase time: 2ms (typ)
- Status Register
- Electronic Signature
- Chip Enable ‘don’t care’
  - for simple interface with microcontroller
- Serial Number option



TSOP48 12 x 20mm

- Data protection
  - Hardware and Software Block Locking
  - Hardware Program/Erase locked during Power transitions
- Data integrity
  - 100,000 Program/Erase cycles
  - 10 years Data Retention
- ECOPACK® package
- Development tools
  - Error Correction Code software and hardware models
  - Bad Blocks Management and Wear Leveling algorithms
  - File System OS Native reference software
  - Hardware simulation models

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Summary description

The NAND Flash 2112 Byte/ 1056 Word Page is a family of non-volatile Flash memories that uses NAND cell technology. The NAND04GW3B2B and NAND08GW3B2A have a density of 4 Gbits and 8 Gbits, respectively. They operate from a 3V voltage supply. The size of a Page is 2112 Bytes (2048 + 64 spare).

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC).

The device has hardware and software security features:

- A Write Protect pin is available to give a hardware protection against program and erase operations.
- A Block Locking scheme is available to provide user code and/or data protection.

The device features an open-drain Ready/Busy output that can be used to identify if the Program/Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back Program command is available to optimize the management of defective blocks. When a Page Program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

The NAND04GW3B2B and NAND08GW3B2A have Cache Program and Cache Read features which improve the program and read throughputs for large files. During Cache Programming, the device loads the data in a Cache Register while the previous data is transferred to the Page Buffer and programmed into the memory array. During Cache Reading, the device loads the data in a Cache Register while the previous data is transferred to the I/O Buffers to be read.

The device has the Chip Enable Don’t Care feature, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation.

The devices have the option of a Unique Identifier (serial number), which allows each device to be uniquely identified.

The Unique Identifier options is subject to an NDA (Non Disclosure Agreement) and so not described in the datasheet. For more details of this option contact your nearest ST Sales office.

The device is available in a TSOP48 (12 x 20mm) package. In order to meet environmental requirements, ST offers the NAND04GW3B2B and NAND08GW3B2A in ECOPACK® package. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

For information on how to order these options refer to *Table 23: Ordering Information Scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See *Table 1: Product Description*, for all the devices available in the family.

Table 1. Product Description

Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings				Package
							Random access time (max)	Sequential access time (min)	Page Program (typ)	Block Erase (typ)	
NAND04GW3B2B	4 Gb	x8	2048+64 Bytes	128K+4K Bytes	64 Pages x 4096 Blocks	2.7 to 3.6V	25µs	30ns	200µs	2ms	TSOP48
NAND08GW3B2A	8 Gb	x8			64 Pages x 8192 Blocks		25µs	30ns	200µs	2ms	TSOP48 (1)

1. The NAND08GW3B2A is composed of two 4 Gbit dice.

Figure 1. Logic Block Diagram

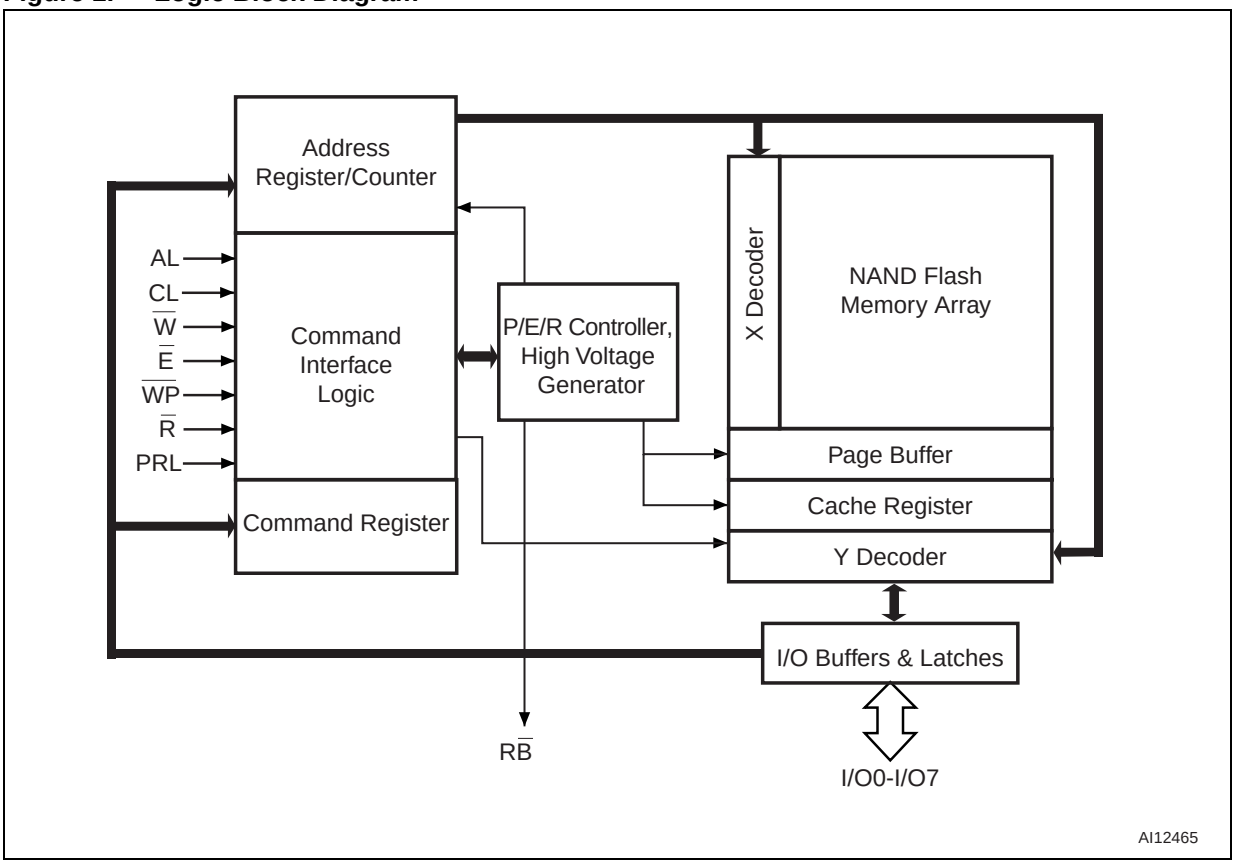


Figure 2. Logic Diagram

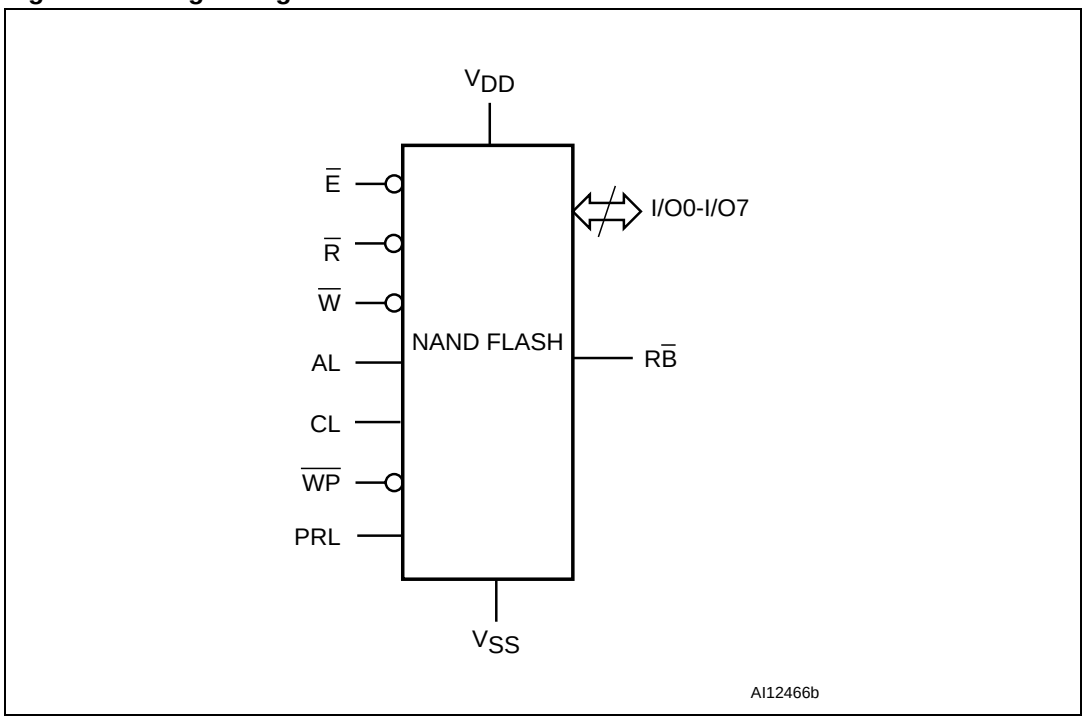
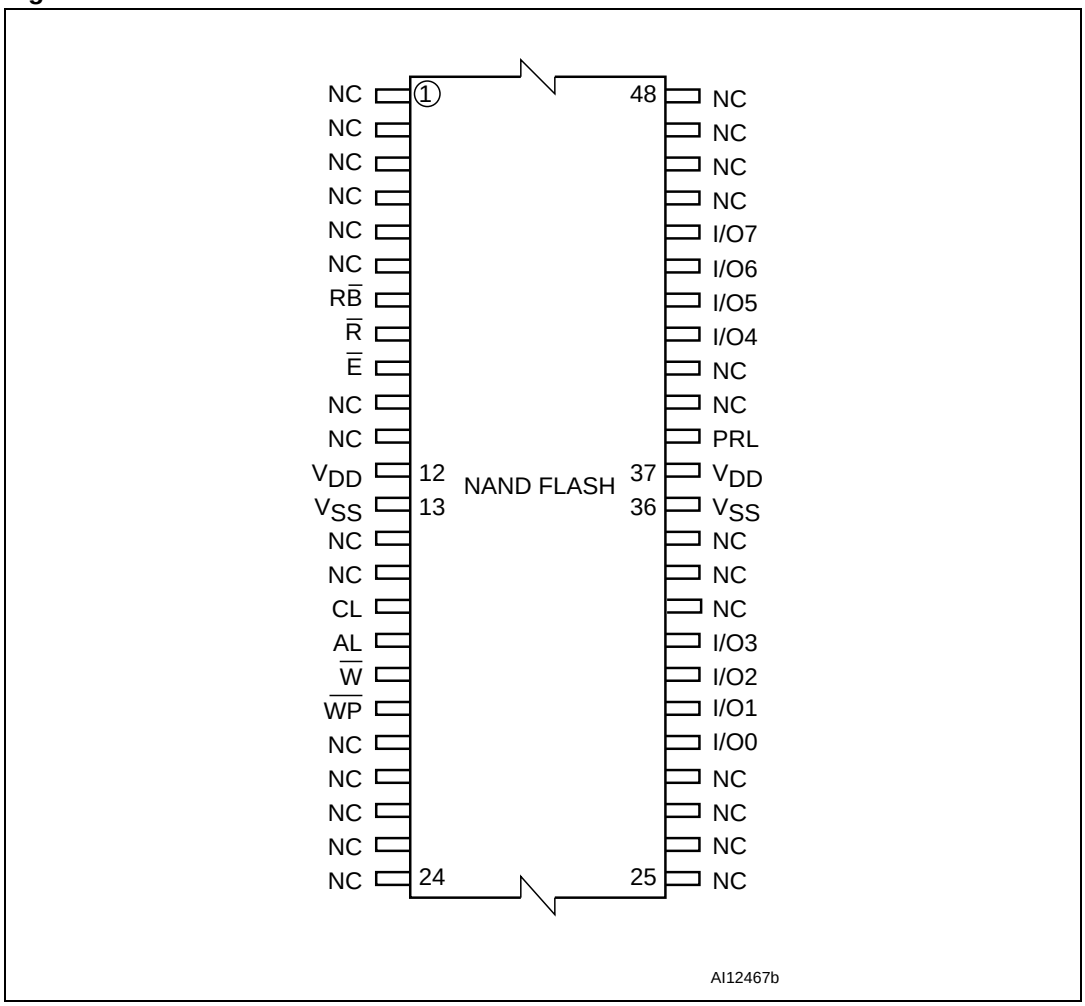


Table 2. Signal Names

I/O0-7	Data Input/Outputs, Address Inputs, or Command Inputs
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}$	Chip Enable
$\overline{R}$	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
PRL	Power-Up Read Enable, Lock/Unlock Enable
V_{DD}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use

Figure 3. TSOP48 Connections



2 Memory array organization

The memory array is made up of NAND structures where 32 cells are connected in series.

The memory array is organized in blocks where each block contains 64 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store Error correction Codes, software flags or Bad Block identification.

The pages are split into a 2048 Byte main area and a spare area of 64 Bytes. Refer to *Figure 4: Memory Array Organization*.

2.1 Bad Blocks

The NAND Flash 2112 Byte/ 1056 Word Page devices may contain Bad Blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional Bad Blocks may develop during the lifetime of the device.

The Bad Block Information is written prior to shipping (refer to *Section 8.1: Bad Block Management* for more details).

Table 3 shows the minimum number of valid blocks. The values shown include both the Bad Blocks that are present when the device is shipped and the Bad Blocks that could develop later on.

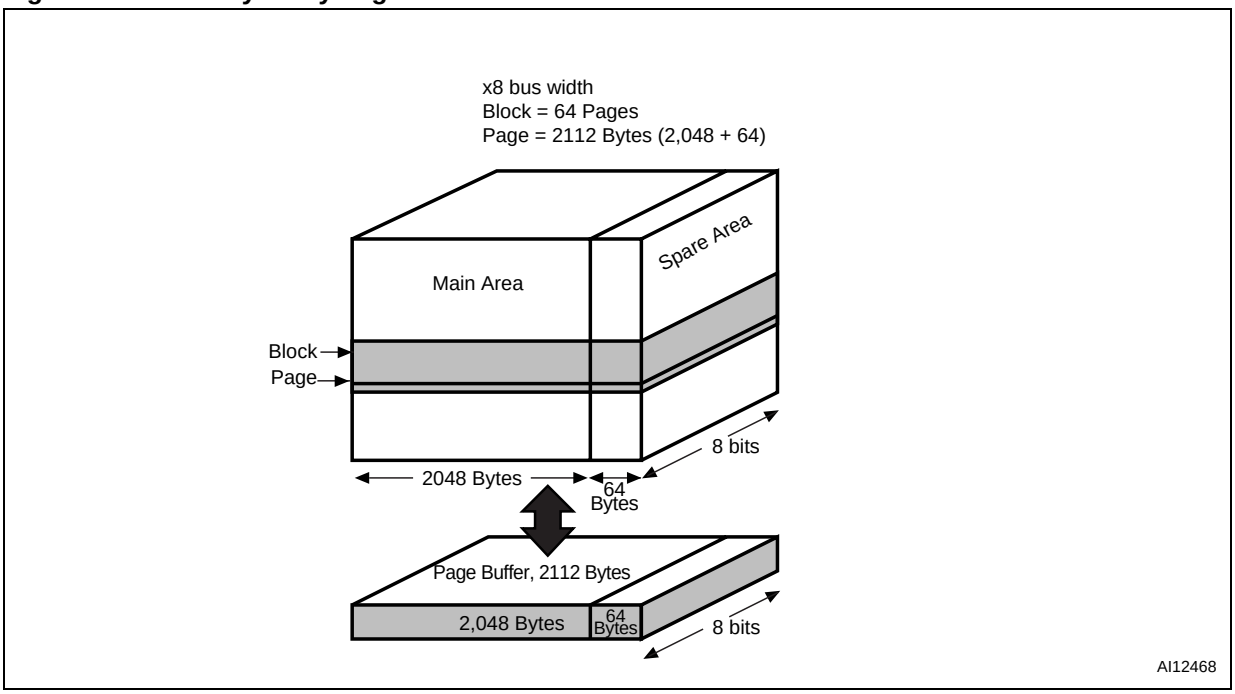
These blocks need to be managed using Bad Blocks Management, Block Replacement or Error Correction Codes (refer to *Section 8: Software algorithms*).

Table 3. Valid Blocks

Density of Device	Min	Max
4 Gbits	4016	4096
8 Gbits(1)	8032	8192

1. The NAND08GW3B2A is composed of two 4 Gbit dice.

Figure 4. Memory Array Organization



3 Signal descriptions

See *Figure 2: Logic Diagram*, and *Table 2: Signal Names*, for a brief overview of the signals connected to this device.

3.1 Inputs/Outputs (I/O0-I/O7)

Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

3.4 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes high, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.5 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.6 Power-Up Read Enable, Lock/Unlock Enable (PRL)

The Power-Up Read Enable, Lock/Unlock Enable input, PRL, is used to enable and disable the lock mechanism. When PRL is High, V_{IH}, the device is in Block Lock mode.

If the Power-Up Read Enable, Lock/Unlock Enable input is not required, the PRL pin should be left unconnected (Not Connected) or connected to V_{SS}.

3.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

3.8 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the *Section 11.1: Ready/Busy Signal Electrical Characteristics* for details on how to calculate the value of the pull-up resistor.

3.10 V_{DD} Supply Voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 19*) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents

3.11 V_{SS} Ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 4: Bus Operations*, for a summary.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command Input

Command Input bus operations are used to give commands to the memory.

The Commands are input on I/O0-I/O7. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

See *Figure 21* and *Table 20* for details of the timings requirements.

4.2 Address Input

Address Input bus operations are used to input the memory addresses.

Addresses are input on I/O0-I/O7. Five bus cycles are required to input the addresses (refer to *Table 5: Address Insertion*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

See *Figure 22* and *Table 20* for details of the timings requirements.

4.3 Data Input

Data Input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 23* and *Table 20* and *Table 21* for details of the timings requirements.

4.4 Data Output

Data Output bus operations are used to read: the data in the memory array, the Status Register, the lock status, the Electronic Signature and the Unique Identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

See *Figure 24* and *Table 21* for details of the timings requirements.

4.5 Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

4.6 Standby

When Chip Enable is High the memory enters Standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 4. Bus Operations

Bus Operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7
Command Input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(1)	Command
Address Input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address
Data Input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data Input
Data Output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data Output
Write Protect	X	X	X	X	X	V_{IL}	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X

1. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 5. Address Insertion

Bus Cycle(1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A30(2)	A29	A28

1. Any additional address input cycles will be ignored.
2. A30 is only valid for the NAND08GW3B2A.

Table 6. Address Definition

Address	Definition
A0 - A11	Column Address
A12 - A17	Page Address
A18 - A29	Block Address (NAND04GW3B2B)
A18 - A30	Block Address (NAND08GW3B2A)

5 Command set

All bus write operations to the device are interpreted by the Command Interface. The Commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The Commands are summarized in *Table 7*.

Table 7. Commands

Command	Bus Write Operations(1)				Commands accepted during busy
	1st cycle	2nd cycle	3rd cycle	4th cycle	
Read	00h(2)	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read	00h	31h	–	–	
Exit Cache Read	34h	–	–	–	Yes(3)
Page Program (Sequential Input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Copy Back Program	00h	35h	85h	10h	
Cache Program	80h	15h	–	–	
Block Erase	60h	D0h	–	–	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes
Read Block Lock Status	7Ah	–	–	–	
Blocks Unlock	23h	24h	–	–	
Blocks Lock	2Ah	–	–	–	
Blocks Lock-Down	2Ch	–	–	–	

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. For consecutive Read operations the 00h command does not need to be repeated.
3. Only during Cache Read busy.

6 Device operations

The following section gives the details of the device operations.

6.1 Read Memory Array

At Power-Up the device defaults to Read mode. To enter Read mode from another mode the Read command must be issued, see *Table 7: Commands*. Once a Read command is issued, subsequent consecutive Read commands only require the confirm command code (30h).

Once a Read command is issued two types of operations are available: Random Read and Page Read.

6.1.1 Random Read

Each time the Read command is issued the first read is Random Read.

6.1.2 Page Read

After the first Random Read access, the page data (2112 Bytes) are transferred to the Page Buffer in a time of t_{WHBH} (refer to *Table 21* for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of the consecutive sequential data, by issuing a **Random Data Output command**.

The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command.

The Random Data Output command can be issued as many times as required within a page.

The Random Data Output command is not accepted during Cache Read operations.

Figure 5. Read Operations

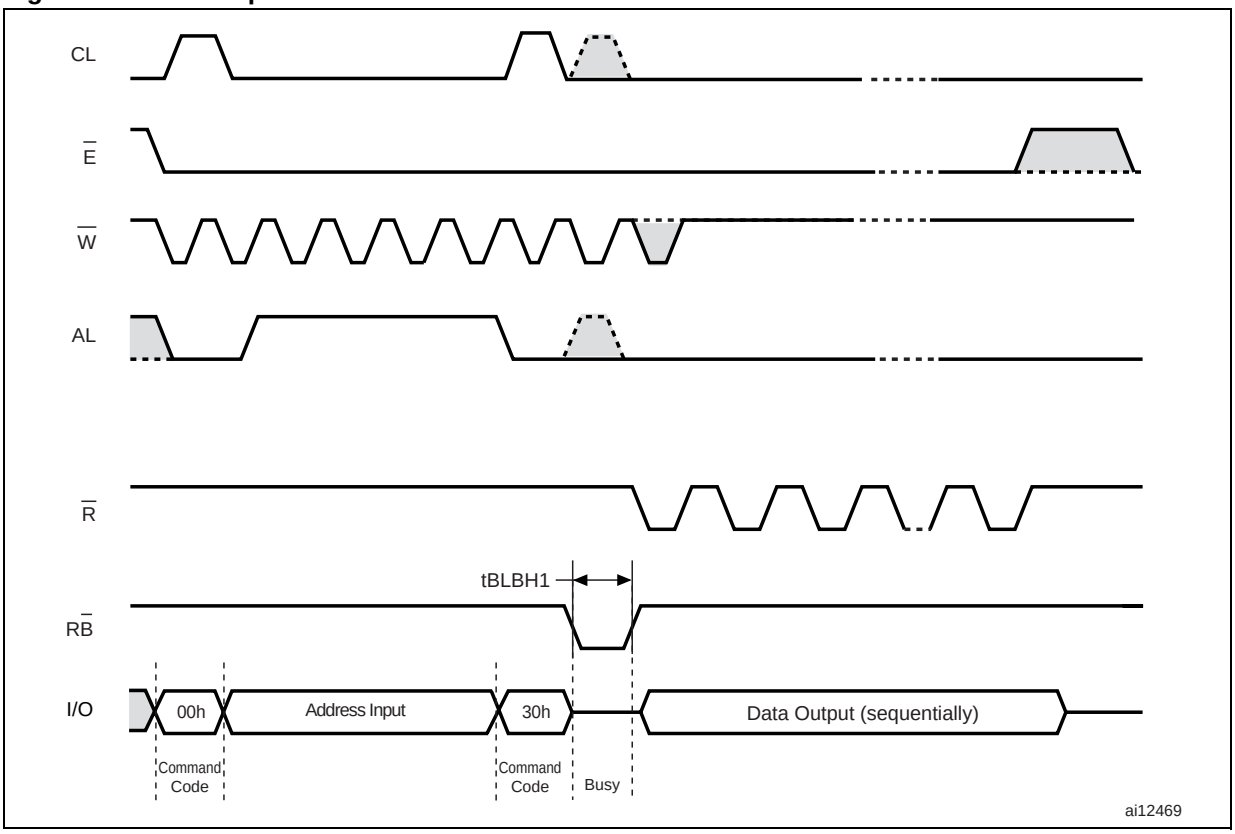
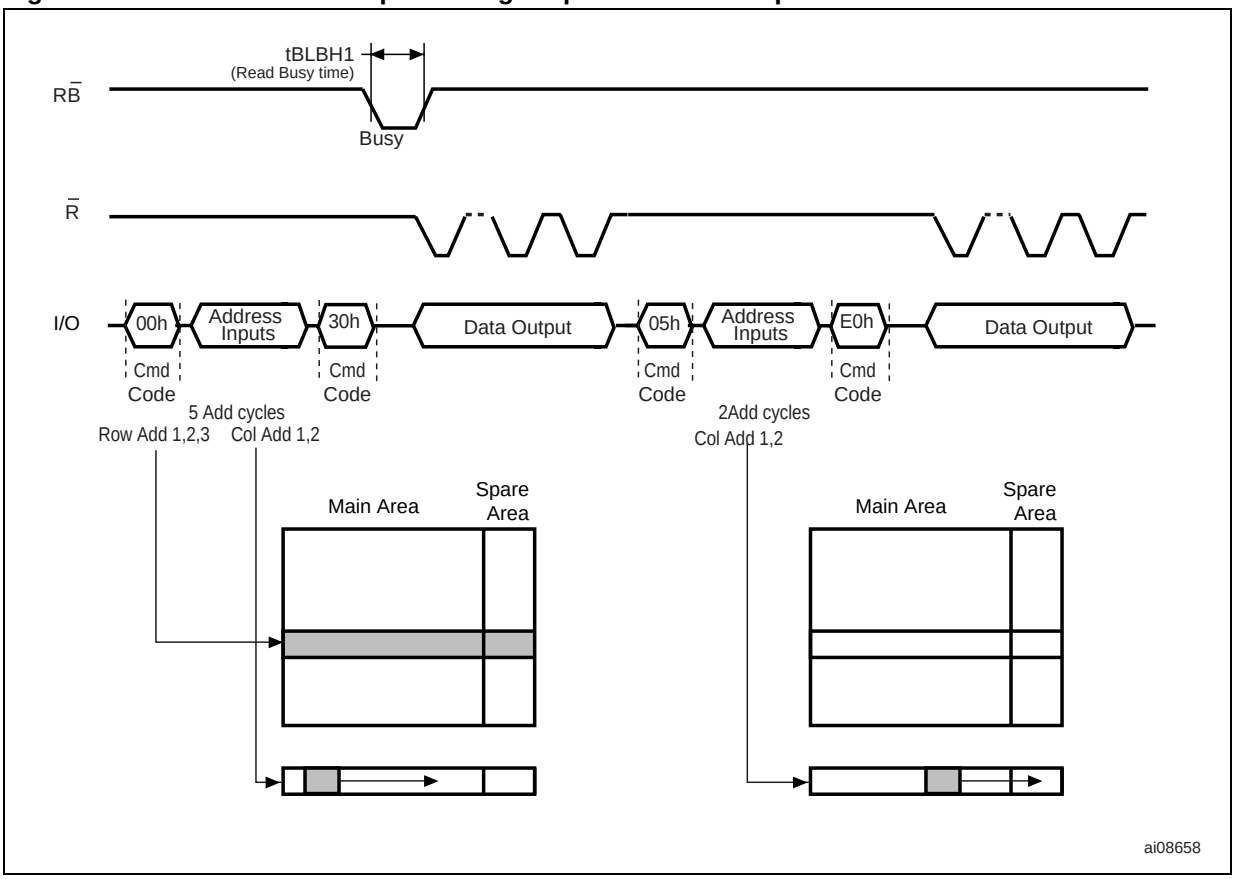


Figure 6. Random Data Output During Sequential Data Output



6.2 Cache Read

The Cache Read operation is used to improve the read throughput by reading data using the Cache Register. As soon as the user starts to read one page, the device automatically loads the next page into the Cache Register.

An Cache Read operation consists of three steps (see *Table 7: Commands*):

1. One bus cycle is required to setup the Cache Read command (the same as the standard Read command).
2. Five (refer to *Table 5: Address Insertion*) bus cycles are then required to input the Start Address.
3. One bus cycle is required to issue the Cache Read confirm command to start the P/E/R Controller.

The Start Address must be at the beginning of a page (Column Address = 00h, see *Table 6: Address Definition*). This allows the data to be output uninterrupted after the latency time (t_{BLBH1}), see *Figure 7: Cache Read Operation*.

The Ready/Busy signal can be used to monitor the start of the operation. During the latency period the Ready/Busy signal goes Low, after this the Ready/Busy signal goes High, even if the device is internally downloading page n+1.

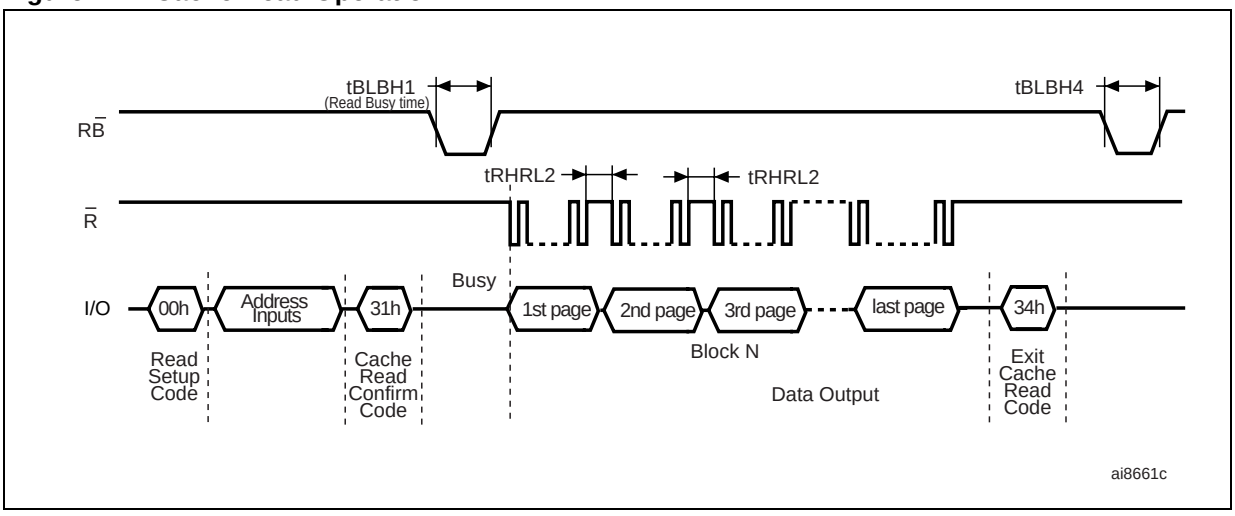
Once the Cache Read operation has started, the Status Register can be read using the Read Status Register command.

During the operation, SR5 can be read, to find out whether the internal reading is ongoing (SR5 = '0'), or has completed (SR5 = '1'), while SR6 indicates whether the Cache Register is ready to download new data.

To exit the Cache Read operation an Exit Cache Read command must be issued (see *Table 7: Commands*).

If the Exit Cache Read command is issued while the device is internally reading page n+1, page n will still be output, but not page n+1.

Figure 7. Cache Read Operation



6.3 Page Program

The Page Program operation is the standard operation to program data to the memory array. Generally, the page is programmed sequentially, however the device does support Random Input within a page.

It is recommended to address pages sequentially within a given block.

The memory array is programmed by page, however partial page programming is allowed where any number of Bytes (1 to 2112) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is four. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

6.3.1 Sequential Input

To input data sequentially the addresses must be sequential and remain in one block.

For Sequential Input each Page Program operation consists of five steps (see *Figure 8: Page Program Operation*):

1. One bus cycle is required to setup the Page Program (Sequential Input) command (see *Table 7: Commands*).
2. Five bus cycles are then required to input the program address (refer to *Table 5: Address Insertion*).
3. The data is then loaded into the Data Registers.
4. One bus cycle is required to issue the Page Program confirm command to start the P/E/R Controller. The P/E/R will only start if the data has been loaded in step 3.
5. the P/E/R Controller then programs the data into the array.

6.3.2 Random Data Input in page

During a Sequential Input operation, the next sequential address to be programmed can be replaced by a random address, by issuing a Random Data Input command. The following two steps are required to issue the command:

1. One bus cycle is required to setup the Random Data Input command (see *Table 7: Commands*)
2. Two bus cycles are then required to input the new column address (refer to *Table 5: Address Insertion*)

Random Data Input can be repeated as often as required in any given page.

Once the program operation has started the Status Register can be read using the Read Status Register command. During program operations the Status Register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R Controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in Read Status Register mode until another valid command is written to the Command Interface.

Figure 8. Page Program Operation

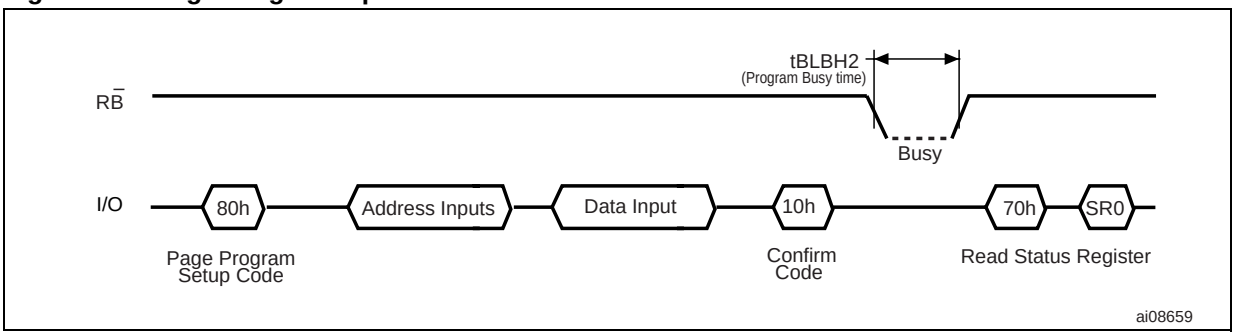
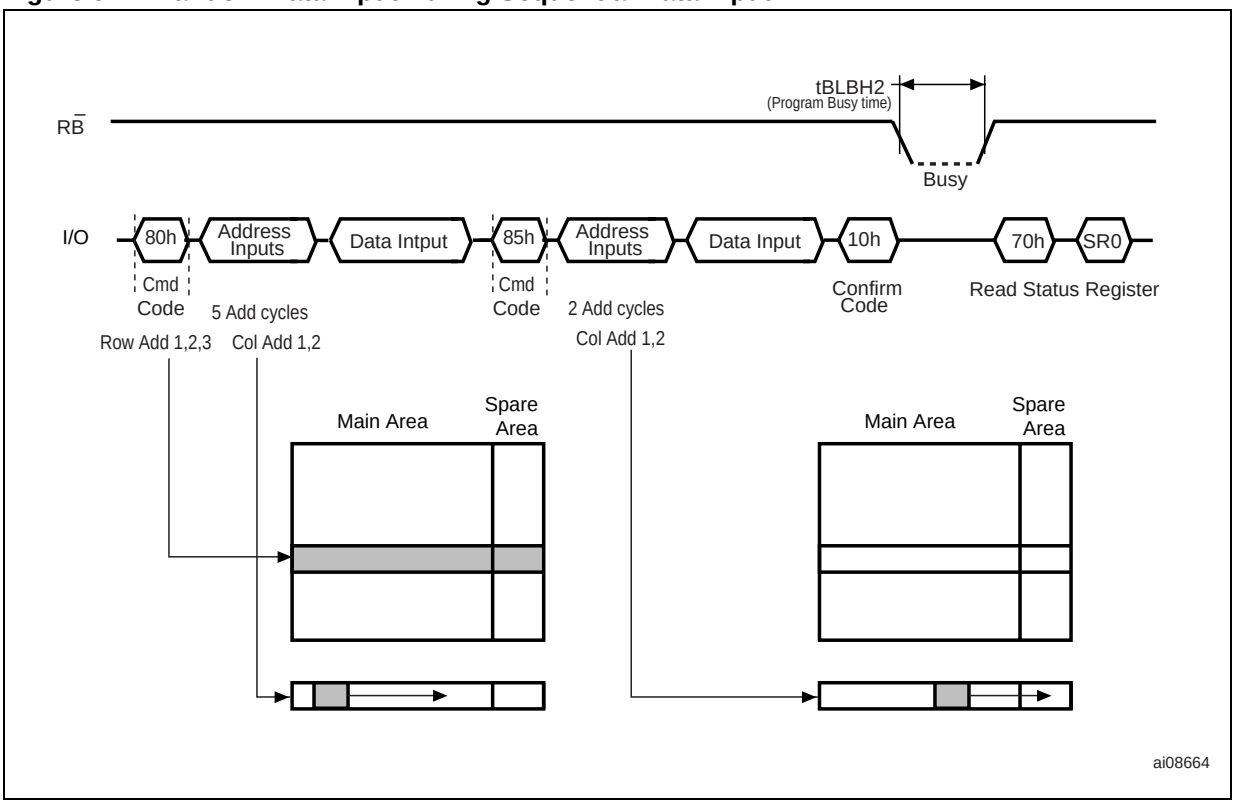


Figure 9. Random Data Input During Sequential Data Input



6.4 Copy Back Program

The Copy Back Program operation is used to copy the data stored in one page and reprogram it in another page.

The Copy Back Program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the Copy Back Program operation fails an error is signalled in the Status Register. However as the standard external ECC cannot be used with the Copy Back Program operation bit error due to charge loss cannot be detected. For this reason it is recommended to limit the number of Copy Back Program operations on the same data and or to improve the performance of the ECC.

The Copy Back Program operation requires four steps:

1. The first step reads the source page. The operation copies all 2112 Bytes from the page into the Data Buffer. It requires:
   - One bus write cycle to setup the command
   - 5 bus write cycles to input the source page address
   - One bus write cycle to issue the confirm command code
2. When the device returns to the ready state (Ready/Busy High), the next bus write cycle of the command is given with the 5 bus cycles to input the target page address. See *Table 8* for the addresses that must be the same for the source and target page.
3. Then the confirm command is issued to start the P/E/R Controller.

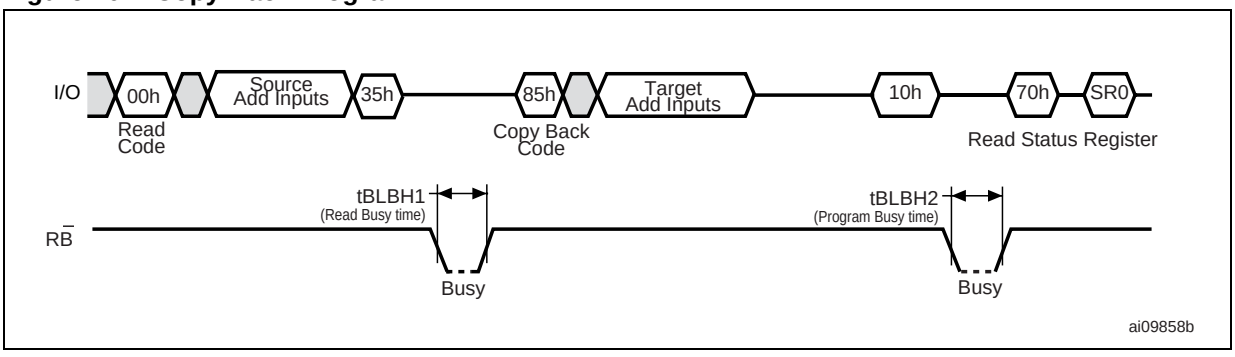
To see the Data Input cycle for modifying the source page and an example of the Copy Back Program operation refer to *Figure 10: Copy Back Program*.

A data input cycle to modify a portion or a multiple distant portion of the source page, is shown in *Figure 11: Page Copy Back Program with Random Data Input*.

Table 8. Copy Back Program addresses

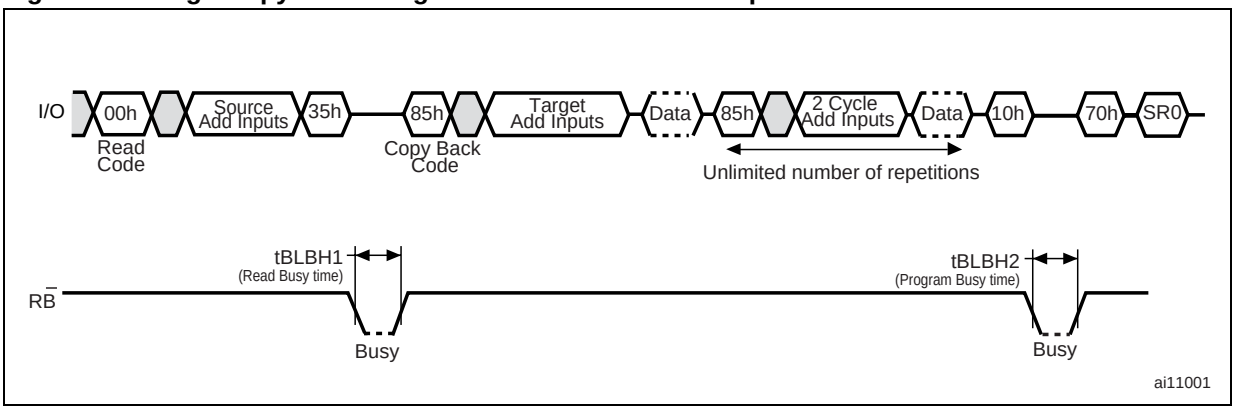
Density	Source and target page addresses
4 Gbits	no constraint
8 Gbits	same A30

Figure 10. Copy Back Program



1. Copy back program is only permitted between odd address pages or even address pages.

Figure 11. Page Copy Back Program with Random Data Input



6.5 Cache Program

The Cache Program operation is used to improve the programming throughput by programming data using the Cache Register. The Cache Program operation can only be used within one block. The Cache Register allows new data to be input while the previous data that was transferred to the Page Buffer is programmed into the memory array.

The following sequence is required to perform a Cache Program operation (refer to *Figure 12: Cache Program Operation*):

1. First of all the program setup command is issued (one bus cycle to issue the program setup command then five bus write cycles to input the address), the data is then input (up to 2112 Bytes) and loaded into the Cache Register.
2. One bus cycle is required to issue the confirm command to start the P/E/R Controller.
3. The P/E/R Controller then transfers the data to the Page Buffer. During this the device is busy for a time of t_{WHBH2}.
4. Once the data is loaded into the Page Buffer the P/E/R Controller programs the data into the memory array. As soon as the Cache Registers are empty (after t_{WHBH2}) a new Cache program command can be issued, while the internal programming is still executing.

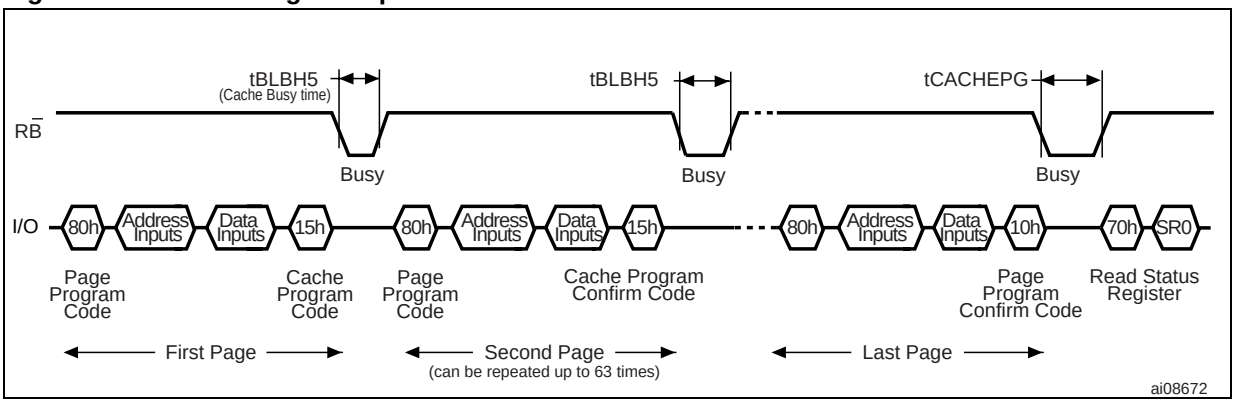
Once the program operation has started the Status Register can be read using the Read Status Register command. During Cache Program operations SR5 can be read to find out whether the internal programming is ongoing (SR5 = '0') or has completed (SR5 = '1') while SR6 indicates whether the Cache Register is ready to accept new data. If any errors have been detected on the previous page (Page N-1), the Cache Program Error Bit SR1 will be set to '1', while if the error has been detected on Page N the Error Bit SR0 will be set to '1'.

When the next page (Page N) of data is input with the Cache Program command, t_{WHBH2} is affected by the pending internal programming. The data will only be transferred from the Cache Register to the Page Buffer when the pending program cycle is finished and the Page Buffer is available.

If the system monitors the progress of the operation using only the Ready/Busy signal, the last page of data must be programmed with the Page Program confirm command (10h).

If the Cache Program confirm command (15h) is used instead, Status Register bit SR5 must be polled to find out if the last programming is finished before starting any other operations.

Figure 12. Cache Program Operation



1. Up to 64 pages can be programmed in one Cache Program operation.
2. $t_{CACHEPG}$ is the program time for the last page + the program time for the (last –1)th page –(Program command cycle time + Last page data loading time).

6.6 Block Erase

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to '1'. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 13: Block Erase Operation*):

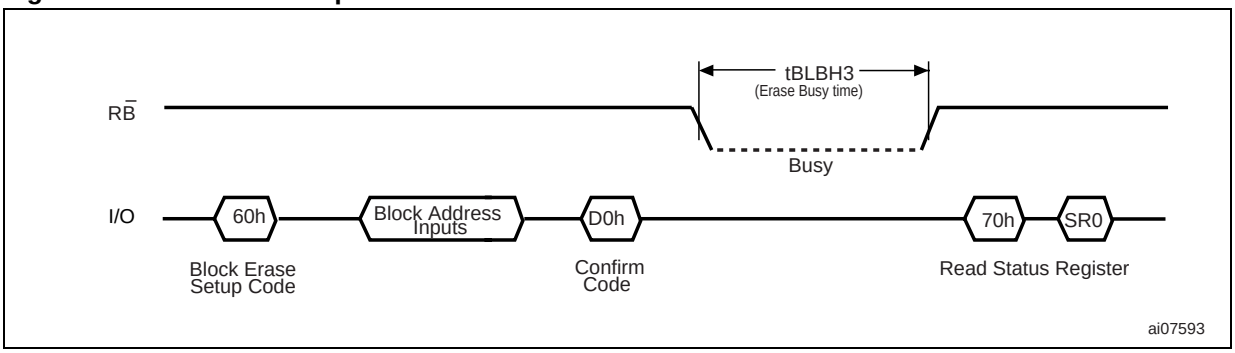
1. One bus cycle is required to setup the Block Erase command. Only addresses A18-A29 are used, the other address inputs are ignored.
2. Three bus cycles are then required to load the address of the block to be erased. Refer to *Table 6: Address Definition* for the block addresses of each device.
3. One bus cycle is required to issue the Block Erase confirm command to start the P/E/R Controller.

The operation is initiated on the rising edge of write Enable, $\overline{W}$, after the confirm command is issued. The P/E/R Controller handles Block Erase and implements the verify process.

During the Block Erase operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R Controller bit SR6 is set to '1' and the Ready/Busy signal goes High. If the operation completed successfully, the Write Status Bit SR0 is '0', otherwise it is set to '1'.

Figure 13. Block Erase Operation



6.7 Reset

The Reset command is used to reset the Command Interface and Status Register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.

If the device has already been reset then the new Reset command will not be accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued, refer to *Table 21* for the values.

6.8 Read Status Register

The device contains a Status Register which provides information on the current or previous Program or Erase operation. The various bits in the Status Register convey information and errors on the operation.

The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the Status Register.

After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued. Therefore if a Read Status Register command is issued during a Random Read cycle a new Read command must be issued to continue with a Page Read operation.

The Status Register bits are summarized in *Table 9: Status Register Bits*,. Refer to *Table 9: Status Register Bits* in conjunction with the following text descriptions.

6.8.1 Write Protection Bit (SR7)

The Write Protection bit can be used to identify if the device is protected or not. If the Write Protection bit is set to ‘1’ the device is not protected and program or erase operations are allowed. If the Write Protection bit is set to ‘0’ the device is protected and program or erase operations are not allowed.

6.8.2 P/E/R Controller and Cache Ready/Busy Bit (SR6)

Status Register bit SR6 has two different functions depending on the current operation.

During Cache operations SR6 acts as a Cache Ready/Busy bit, which indicates whether the Cache Register is ready to accept new data. When SR6 is set to '0', the Cache Register is busy and when SR6 is set to '1', the Cache Register is ready to accept new data.

During all other operations SR6 acts as a P/E/R Controller bit, which indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to ‘0’, the P/E/R Controller is active (device is busy); when the bit is set to ‘1’, the P/E/R Controller is inactive (device is ready).

6.8.3 P/E/R Controller Bit (SR5)

The Program/Erase/Read Controller bit indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to ‘0’, the P/E/R Controller is active (device is busy); when the bit is set to ‘1’, the P/E/R Controller is inactive (device is ready).

6.8.4 Cache Program Error Bit (SR1)

The Cache Program Error bit can be used to identify if the previous page (page N-1) has been successfully programmed or not in a Cache Program operation. SR1 is set to ’1’ when

the Cache Program operation has failed to program the previous page (page N-1) correctly. If SR1 is set to ‘0’ the operation has completed successfully.

The Cache Program Error bit is only valid during Cache Program operations, during other operations it is Don’t Care.

6.8.5 Error Bit (SR0)

The Error bit is used to identify if any errors have been detected by the P/E/R Controller. The Error Bit is set to ’1’ when a program or erase operation has failed to write the correct data to the memory. If the Error Bit is set to ‘0’ the operation has completed successfully. The Error Bit SR0, in a Cache Program operation, indicates a failure on Page N.

6.8.6 SR4, SR3 and SR2 are Reserved

Table 9. Status Register Bits

Bit	Name	Logic Level	Definition
SR7	Write Protection	'1'	Not Protected
		'0'	Protected
SR6	Program/ Erase/ Read Controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
	Cache Ready/Busy	'1'	Cache Register ready (Cache only)
		'0'	Cache Register busy (Cache only)
SR5	Program/ Erase/ Read Controller(1)	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR4, SR3, SR2	Reserved	Don’t Care	
SR1	Cache Program Error(2)	'1'	Page N-1 failed in Cache Program operation
		'0'	Page N-1 programmed successfully
SR0	Generic Error	‘1’	Error – operation failed
		‘0’	No Error – operation successful
	Cache Program Error	‘1’	Page N failed in Cache Program operation
		‘0’	Page N programmed successfully

1. Only valid for Cache operations, for other operations it is same as SR6.
2. Only valid for Cache Program operations, for other operations it is Don’t Care.

6.9 Read Electronic Signature

The device contains a Manufacturer Code and Device Code. To read these codes three steps are required:

1. One Bus Write cycle to issue the Read Electronic Signature command (90h)
2. One Bus Write cycle to input the address (00h)
3. Four Bus Read Cycles to sequentially output the data (as shown in *Table 10: Electronic Signature*).

Table 10. Electronic Signature

Root Part Number	Byte 1	Byte 2	Byte 3 (see *Table 11*)	Byte 4 (see *Table 12*)
	Manufacturer Code	Device code		
NAND04GW3B2B	20h	DCh	80h	95h
NAND08GW3B2A	20h	D3h	81h	95h

Table 11. Electronic Signature Byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Internal Chip number	0 0 0 1 1 0 1 1	1 2 4 8
I/O3-I/O2	Cell Type	0 0 0 1 1 0 1 1	2-level cell 4-level cell 8-level cell 16-level cell
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 4 8
I/O6	Interleaved Programming between multiple devices	0 1	Not supported Supported
I/O7	Cache Program	0 1	Not supported Supported

Table 12. Electronic Signature Byte 4

I/O	Definition	Value	Description
I/O1-I/O0	Page Size (Without Spare Area)	0 0 0 1 1 0 1 1	1 KBytes 2 KBytes Reserved Reserved
I/O2	Spare Area Size (Byte / 512 Byte)	0 1	8 16
I/O7, I/O3	Minimum sequential access time	0 0 1 0 0 1 1 1	50ns 30ns Reserved Reserved
I/O5-I/O4	Block Size (without Spare Area)	0 0 0 1 1 0 1 1	64 KBytes 128 KBytes 256 KBytes Reserved
I/O6	Organization	0 1	x8 x16

7 Data Protection

The device has both hardware and software features to protect against program and erase operations.

It features a Write Protect, $\overline{WP}$, pin, which can be used to protect the device against program and erase operations. It is recommended to keep $\overline{WP}$ at V_{IL} during power-up and power-down.

In addition, to protect the memory from any involuntary program/erase operations during power-transitions, the device has an internal voltage detector which disables all functions whenever V_{DD} is below V_{LKO} (see *Table 19: DC Characteristics*).

The device features a Block Lock mode, which is enabled by setting the Power-Up Read Enable, Lock/Unlock Enable, PRL, signal to High.

The Block Lock mode has two levels of software protection.

- Blocks Lock/Unlock
- Blocks Lock-down

Refer to *Figure 16: Block Protection State Diagram* for an overview of the protection mechanism.

7.1 Blocks Lock

All the blocks are locked simultaneously by issuing a Blocks Lock command (see *Table 7: Commands*).

All blocks are locked after power-up and when the Write Protect signal is Low.

Once all the blocks are locked, one sequence of consecutive blocks can be unlocked by using the Blocks Unlock command.

Refer to *Figure 21: Command Latch AC Waveforms* for details on how to issue the command.

7.2 Blocks Unlock

A sequence of consecutive locked blocks can be unlocked, to allow program or erase operations, by issuing an Blocks Unlock command (see *Table 7: Commands*).

The Blocks Unlock command consists of four steps:

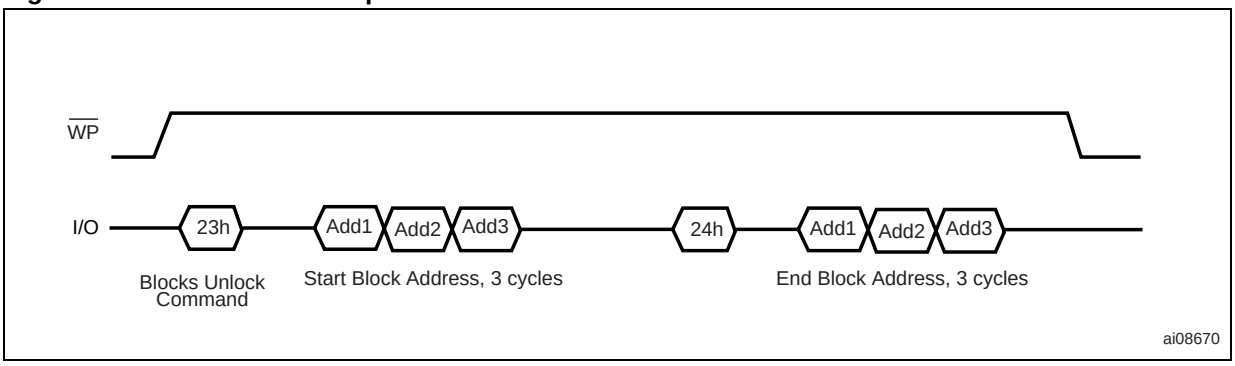
- One bus cycle to setup the command.
- Three bus cycles to give the Start Block Address (refer to *Table 6: Address Definition*, and *Figure 14: Blocks Unlock Operation*).
- One bus cycle to confirm the command.
- Three bus cycles to give the End Block Address (refer to *Table 6: Address Definition*, and *Figure 14: Blocks Unlock Operation*).

The Start Block Address must be nearer the logical LSB (Least Significant Bit) than End Block Address.

If the Start Block Address is the same as the End Block Address, only one block is unlocked.

Only one consecutive area of blocks can be unlocked at any one time. It is not possible to unlock multiple areas.

Figure 14. Blocks Unlock Operation



7.3 Blocks Lock-Down

The Lock-Down feature provides an additional level of protection. A Locked-down block cannot be unlocked by a software command. Locked-Down blocks can only be unlocked by setting the Write Protect signal to Low for a minimum of 100ns.

Only locked blocks can be locked-down. The command has no affect on unlocked blocks.

Refer to *Figure 21: Command Latch AC Waveforms* for details on how to issue the command.

7.4 Block Lock Status

In Block Lock mode (PRL High) the Block Lock Status of each block can be checked by issuing a Read Block Lock Status command (see *Table 7: Commands*).

The command consists of:

- One bus cycle to give the command code
- Three bus cycles to give the block address

After this, a read cycle will then output the Block Lock Status on the I/O pins on the falling edge of Chip Enable or Read Enable, whichever occurs last. Chip Enable or Read Enable do not need to be toggled to update the status.

The Read Block Lock Status command will not be accepted while the device is busy ($R\overline{B}$ Low).

The device will remain in Read Block Lock Status mode until another command is issued.

Figure 15. Read Block Lock Status Operation

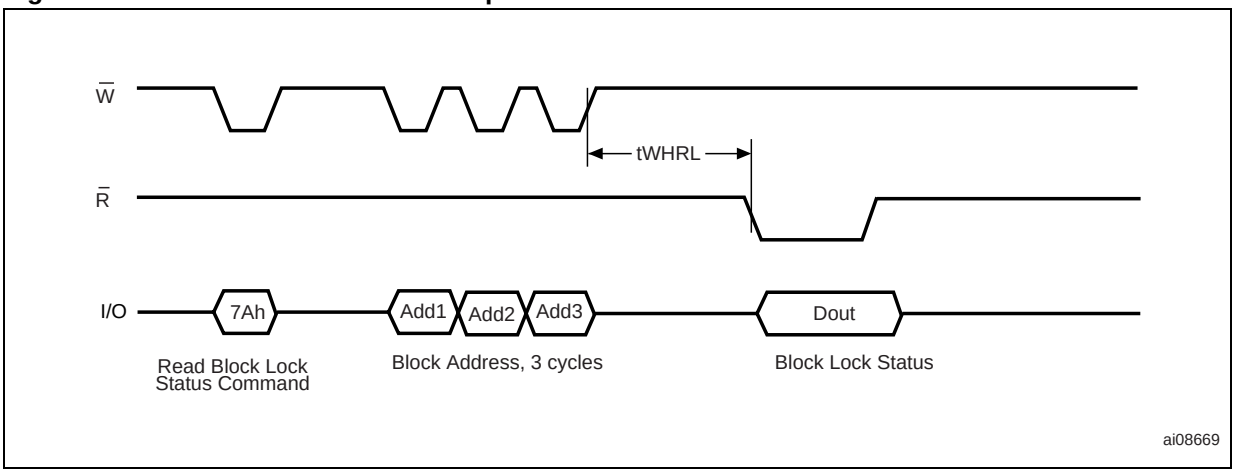
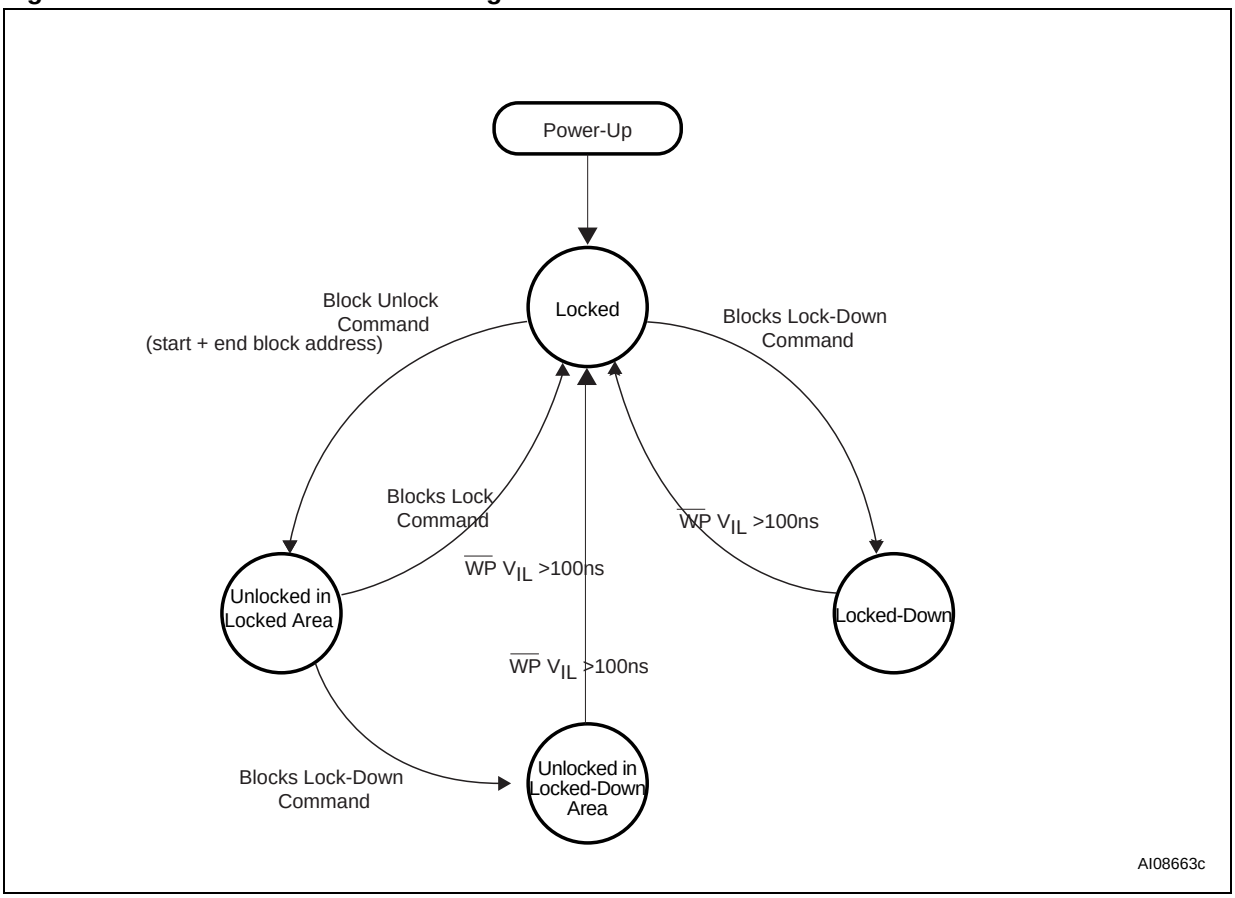


Table 13. Block Lock Status(1)

Status	I/O7-I/O3	I/O2	I/O1	I/O0
Locked	X	0	1	0
Unlocked	X	1	1	0
Locked-Down	X	0	0	1
Unlocked in Locked-Down Area	X	1	0	1

1. X = Don't Care.

Figure 16. Block Protection State Diagram



1. PRL must be High for the software commands to be accepted.

8 Software algorithms

This section gives information on the software algorithms that ST recommends to implement to manage the Bad Blocks and extend the lifetime of the NAND device.

NAND Flash memories are programmed and erased by Fowler-Nordheim tunnelling using a high voltage. Exposing the device to a high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 15: Program, Erase Times and Program Erase Endurance Cycles* for value) and it is recommended to implement Garbage Collection, a Wear-Leveling Algorithm and an Error Correction Code, to extend the number of program and erase cycles and increase the data retention.

To help integrate a NAND memory into an application ST Microelectronics can provide a File System OS Native reference software, which supports the basic commands of file management.

Contact the nearest ST Microelectronics sales office for more details.

8.1 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block, where the 1st and 6th Bytes, or 1st Word, in the spare area of the 1st page, does not contain FFh, is a Bad Block.

The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in *Figure 17: Bad Block Management Flowchart*.

8.2 Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block.

See *Section 6.4: Copy Back Program* for more details.

Refer to *Table 14: Block Failure* for the recommended procedure to follow if an error occurs during an operation.

Table 14. Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC
Read	ECC

Figure 17. Bad Block Management Flowchart

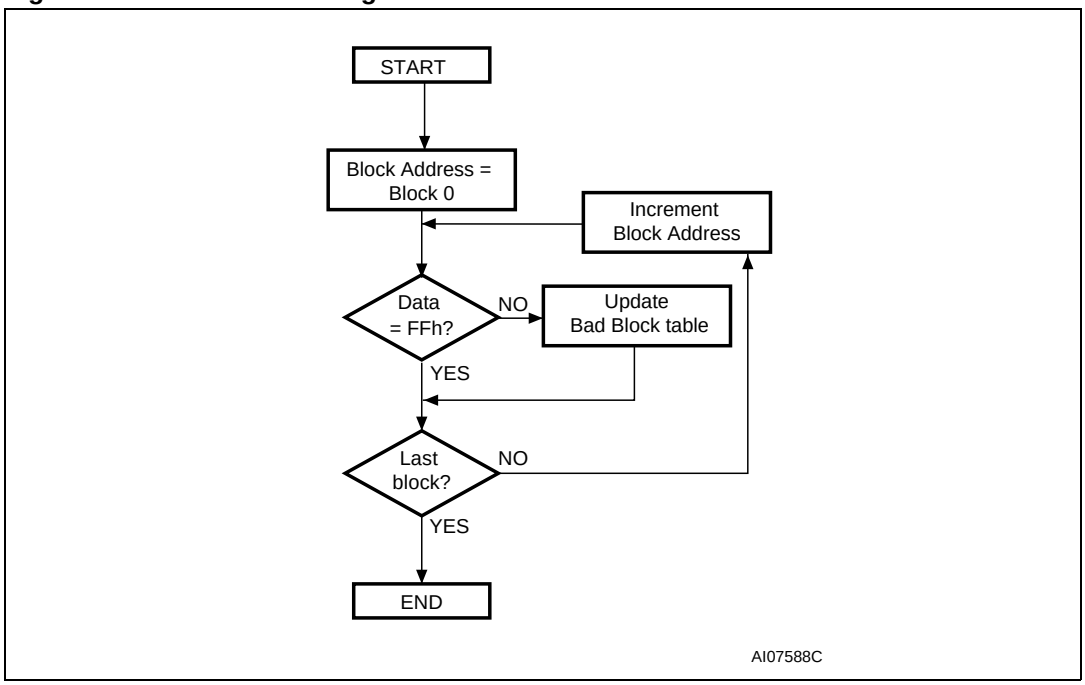
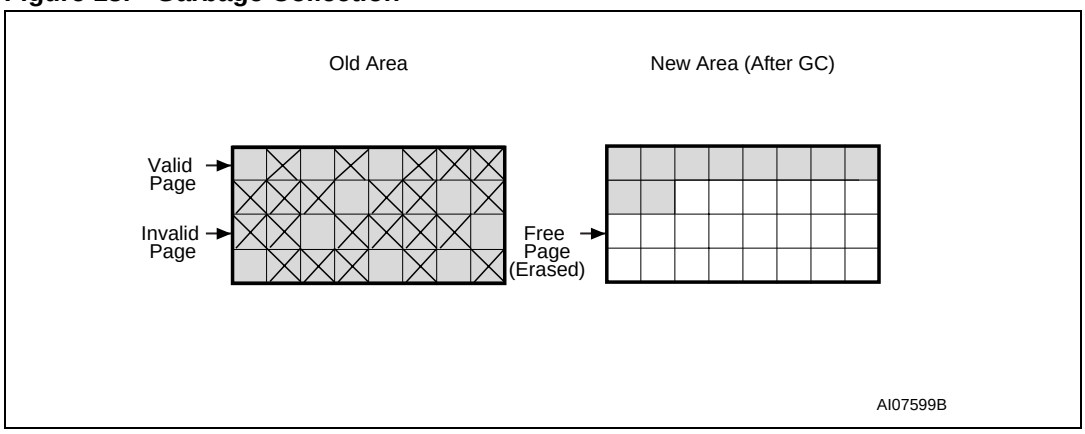


Figure 18. Garbage Collection



8.3 Garbage Collection

When a data page needs to be modified, it is faster to write to the first available page, and the previous page is marked as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations it is recommended to implement a Garbage Collection algorithm. In a Garbage Collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 18: Garbage Collection*).

8.4 Wear-leveling Algorithm

For write-intensive applications, it is recommended to implement a Wear-leveling Algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a Wear-Leveling Algorithm not all blocks get used at the same rate. Blocks with long-lived data do not endure as many write cycles as the blocks with frequently-changed data.

The Wear-leveling Algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

- First Level Wear-leveling, new data is programmed to the free blocks that have had the fewest write cycles.
- Second Level Wear-leveling, long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

The Second Level Wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

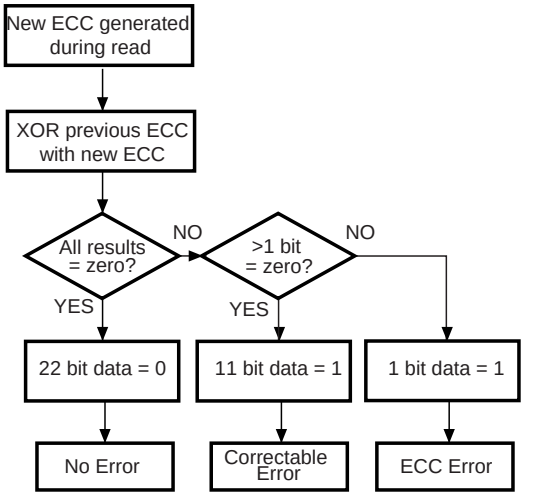
8.5 Error Correction Code

An Error Correction Code (ECC) can be implemented in the NAND Flash memories to identify and correct errors in the data.

For every 2048 bits in the device it is recommended to implement 22 bits of ECC (16 bits for line parity plus 6 bits for column parity).

An ECC model is available in VHDL or Verilog. Contact the nearest ST Microelectronics sales office for more details.

Figure 19. Error Detection



8.6 Hardware simulation models

8.6.1 Behavioral simulation models

Denali Software Corporation models are platform independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND Flash devices, and so allow software to be developed before hardware.

8.6.2 IBIS simulations models

IBIS (I/O Buffer Information Specification) models describe the behavior of the I/O buffers and electrical characteristics of Flash devices.

These models provide information such as AC characteristics, rise/fall times and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

9 Program and Erase times and endurance cycles

The Program and Erase times and the number of Program/ Erase cycles per block are shown in *Table 15*.

Table 15. Program, Erase Times and Program Erase Endurance Cycles

Parameters	NAND Flash			Unit
	Min	**Typ**	Max	
Page Program Time		200	700	µs
Block Erase Time		2	3	ms
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	10			years

10 Maximum rating

Stressing the device above the ratings listed in *Table 16: Absolute Maximum Ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature Under Bias	– 50	125	°C
T_{STG}	Storage Temperature	– 65	150	°C
V_{IO}(1)	Input or Output Voltage	– 0.6	4.6	V
V_{DD}	Supply Voltage	– 0.6	4.6	V

1. Minimum Voltage may undershoot to –2V for less than 20ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2V for less than 20ns during transitions on I/O pins.

11 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 17*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 17. Operating and AC Measurement Conditions

Parameter		NAND Flash		Units
		Min	Max	
Supply Voltage (V_{DD})		2.7	3.6	V
Ambient Temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load Capacitance (C_L) (1 TTL GATE and C_L)		50		pF
Input Pulses Voltages		0	V_{DD}	V
Input and Output Timing Ref. Voltages		$V_{DD}/2$		V
Output Circuit Resistor R_{ref}		8.35		kΩ
Input Rise and Fall Times		5		ns

Table 18. Capacitance(1)

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
$C_{I/O}$	Input/Output Capacitance(2)	V_{IL} = 0V		10	pF

1. T_A = 25°C, f = 1MHz. C_{IN} and $C_{I/O}$ are not 100% tested.
2. Input/output capacitances double in stacked devices.

Figure 20. Equivalent Testing Circuit for AC Characteristics Measurement

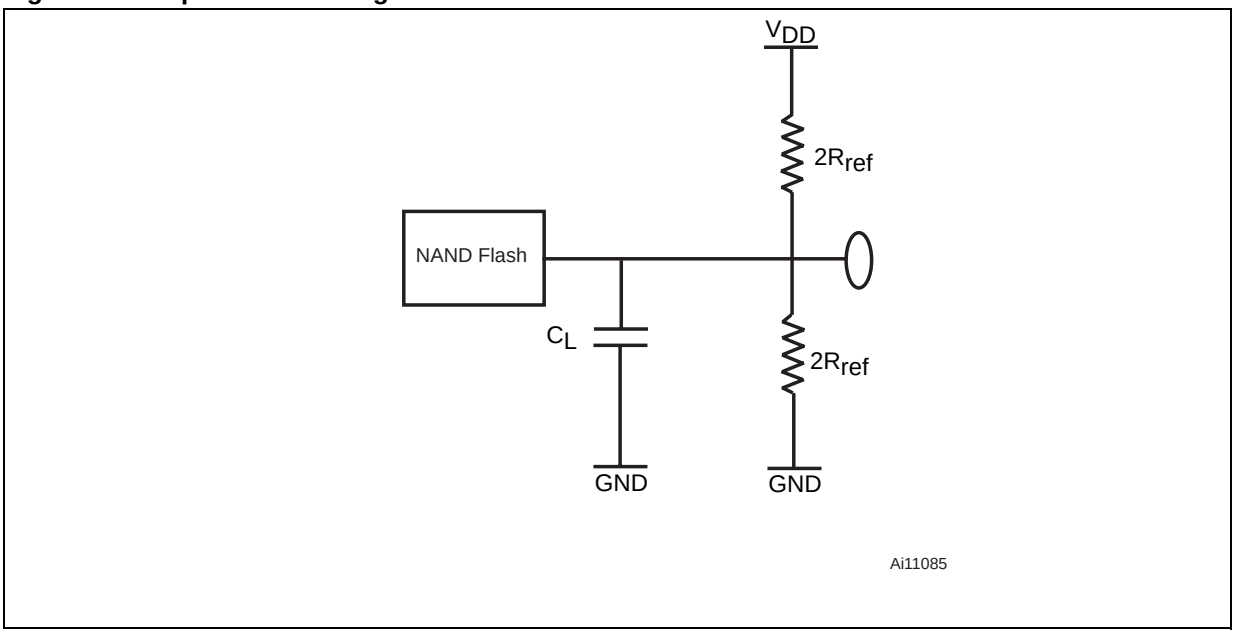


Table 19. DC Characteristics

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{DD1}	Operating Current	Sequential Read	t_{RLRL} minimum $\overline{E}=V_{IL}$, I_{OUT} = 0 mA	-	15	30	mA
I_{DD2}		Program	-	-	15	30	mA
I_{DD3}		Erase	-	-	15	30	mA
I_{DD4}	Standby current (TTL)(1)		E=V_{IH}, $\overline{WP}$=0/V_{DD}			1	mA
I_{DD5}	Standby Current (CMOS)(1)		$\overline{E}$=V_{DD}-0.2, $\overline{WP}$=0/V_{DD}	-	10	50	µA
I_{LI}	Input Leakage Current(1)		V_{IN}= 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output Leakage Current(1)		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input High Voltage		-	0.8V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-	-0.3	-	0.2V_{DD}	V
V_{OH}	Output High Voltage Level		I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output Low Voltage Level		I_{OL} = 2.1mA	-	-	0.4	V
I_{OL} ($R\overline{B}$)	Output Low Current ($R\overline{B}$)		V_{OL} = 0.4V	8	10		mA
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)		-	-	-	1.7	V

1. leakage current and standby current double in stacked devices.

Table 20. AC Characteristics for Command, Address, Data Input

Symbol	Alt. Symbol	Parameter			NAND04GW3B2B, NAND08GW3B2A	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable high	AL Setup time	Min	15	ns
t_{ALHWH}		Address Latch High to Write Enable high				
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable high	CL Setup time	Min	15	ns
t_{CLLWH}		Command Latch Low to Write Enable high				
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data Setup time	Min	15	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable high	$\overline{E}$ Setup time	Min	25	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL Hold time	Min	5	ns
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	5	ns
t_{WHCLL}		Write Enable High to Command Latch Low				
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data Hold time	Min	5	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ Hold time	Min	5	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High Hold time	Min	10	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ Pulse Width	Min	20	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	35	ns

Table 21. AC Characteristics for Operations(1)

Symbol	Alt. Symbol	Parameter			NAND04GW3B2B, NAND08GW3B2A	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read Electronic Signature	Min	15	ns
t_{ALLRL2}			Read cycle	Min	15	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read Busy time	Max	25	µs
t_{BLBH2}	t_{PROG}		Program Busy time	Max	700	µs
t_{BLBH3}	t_{BERS}		Erase Busy time	Max	3	ms
t_{BLBH4}			Reset Busy time, during ready	Max	5	µs
t_{BLBH5}	t_{CBSY}		Cache Busy time	Typ	3	µs
				Max	700	µs
t_{WHBH1}	t_{RST}	Write Enable High to Ready/Busy High	Reset Busy time, during read	Max	5	µs
			Reset Busy time, during program	Max	10	µs
			Reset Busy time, during erase	Max	500	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	15	ns

Table 21. AC Characteristics for Operations(1) (continued)

t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	50	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-z		Max	50	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	30	ns
t_{RHRL1}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	Min	10	ns
t_{EHQX}	t_{COH}	Chip Enable high to Output Hold		Min	15	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable Pulse Width	Min	15	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read Cycle time	Min	30	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable Access time	Max	25	ns
			Read ES Access time(2)			
t_{WHBH}	t_R	Write Enable High to Ready/Busy High	Read Busy time	Max	25	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	60	ns
t_{RHRL2}	t_{CRRH}	Read Enable High hold time during Cache Read operation		Min	100	ns
t_{WHWH}	t_{ADL}(3)	Last Address latched to Data Loading Time during Program operations		Min	100	ns
t_{VHWH} t_{VLWH}	t_{WW}(4)	Write Protection time		Min	100	ns

1. The time to Ready depends on the value of the pull-up resistor tied to the Ready/Busy pin. See *Figure 33*, *Figure 34* and *Figure 35*.
2. ES = Electronic Signature.
3. t_{ADL} is the time from $\overline{W}$ rising edge during the final address cycle to $\overline{W}$ rising edge during the first data cycle.
4. During a Program/Erase Enable Operation, t_{WW} is the delay from $\overline{WP}$ high to $\overline{W}$ High.
   During a Program/Erase Disable Operation, t_{WW} is the delay from $\overline{WP}$ Low to $\overline{W}$ High.

Figure 21. Command Latch AC Waveforms

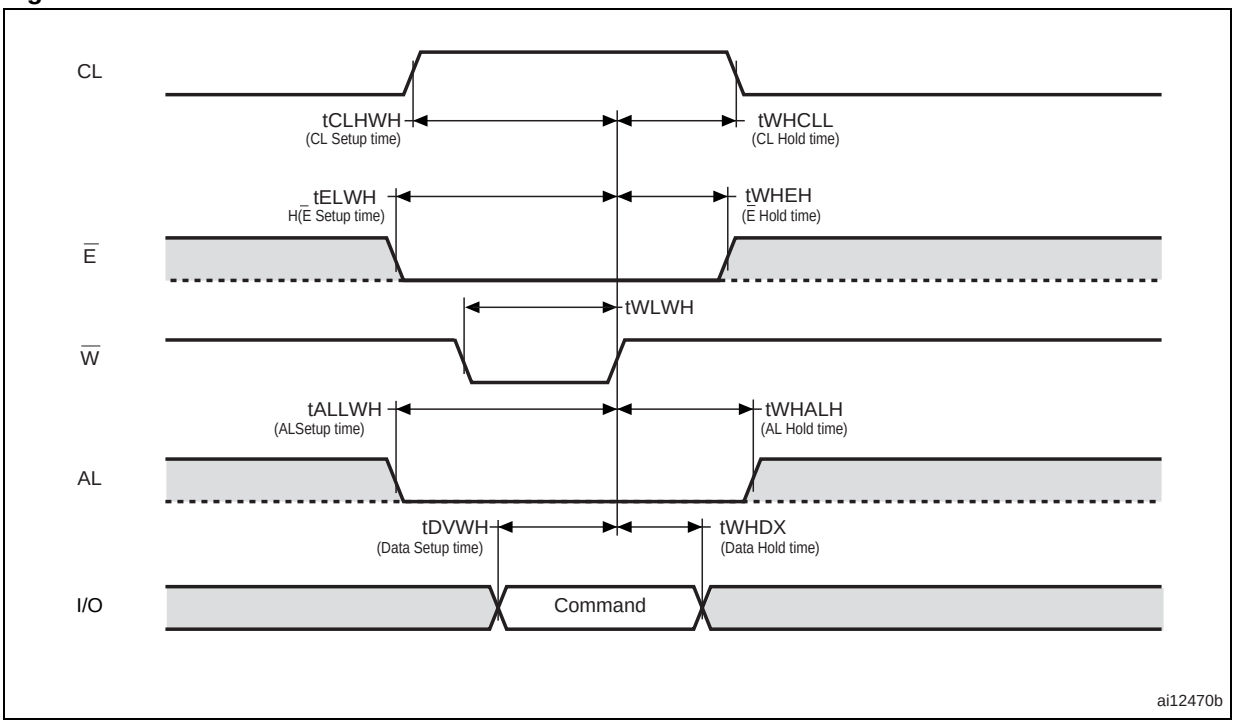


Figure 22. Address Latch AC Waveforms

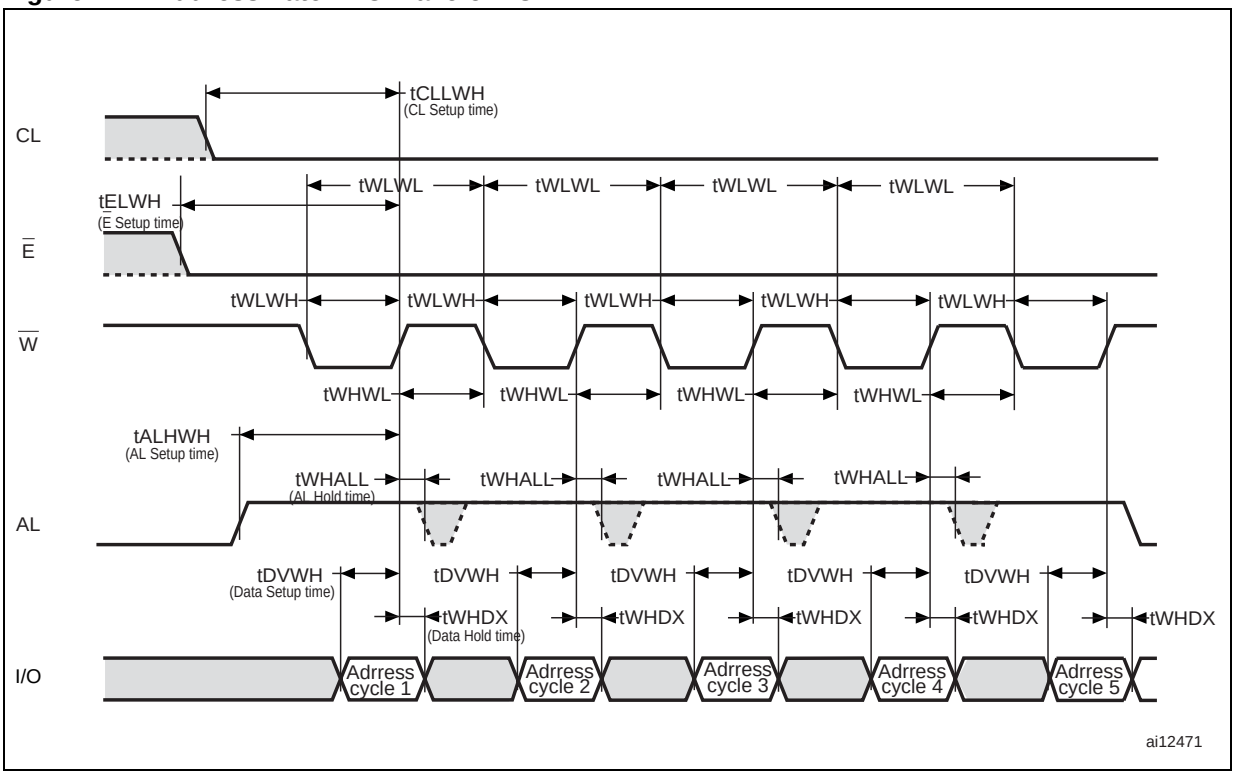
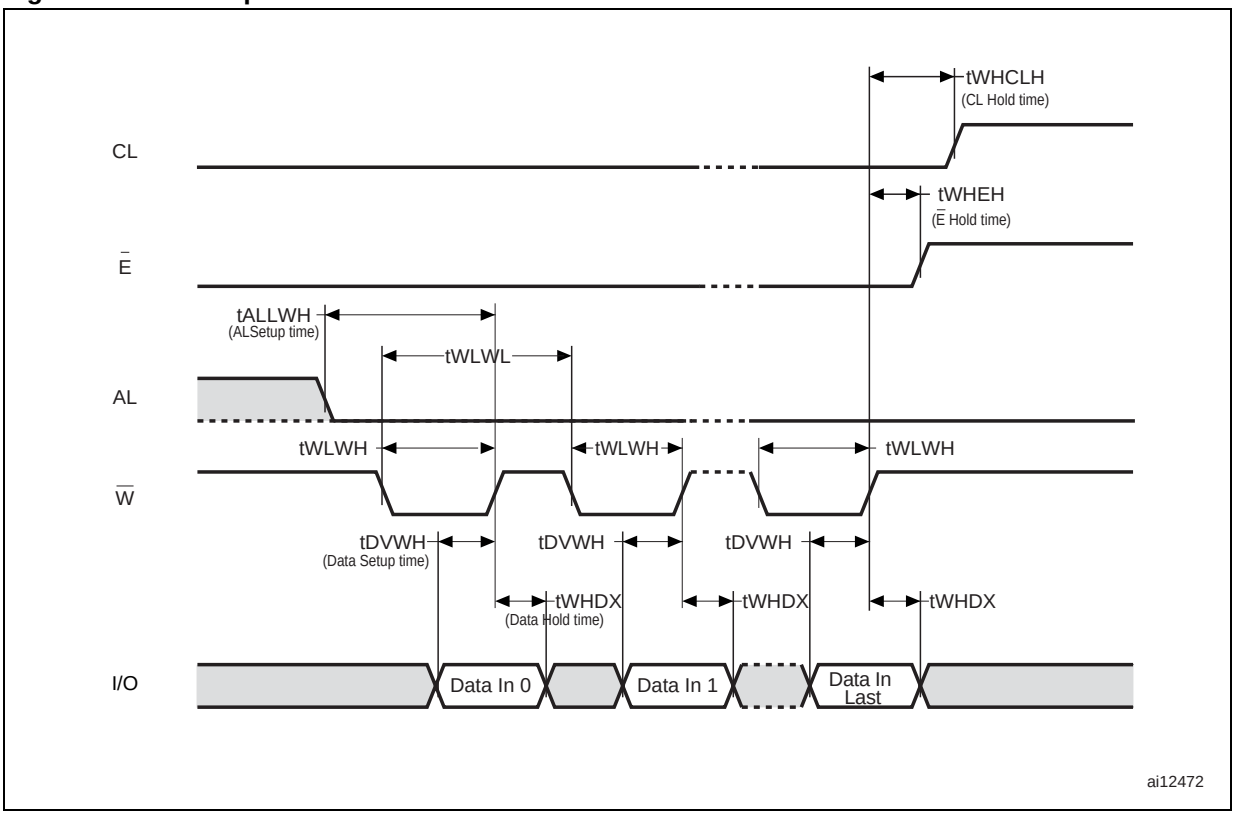
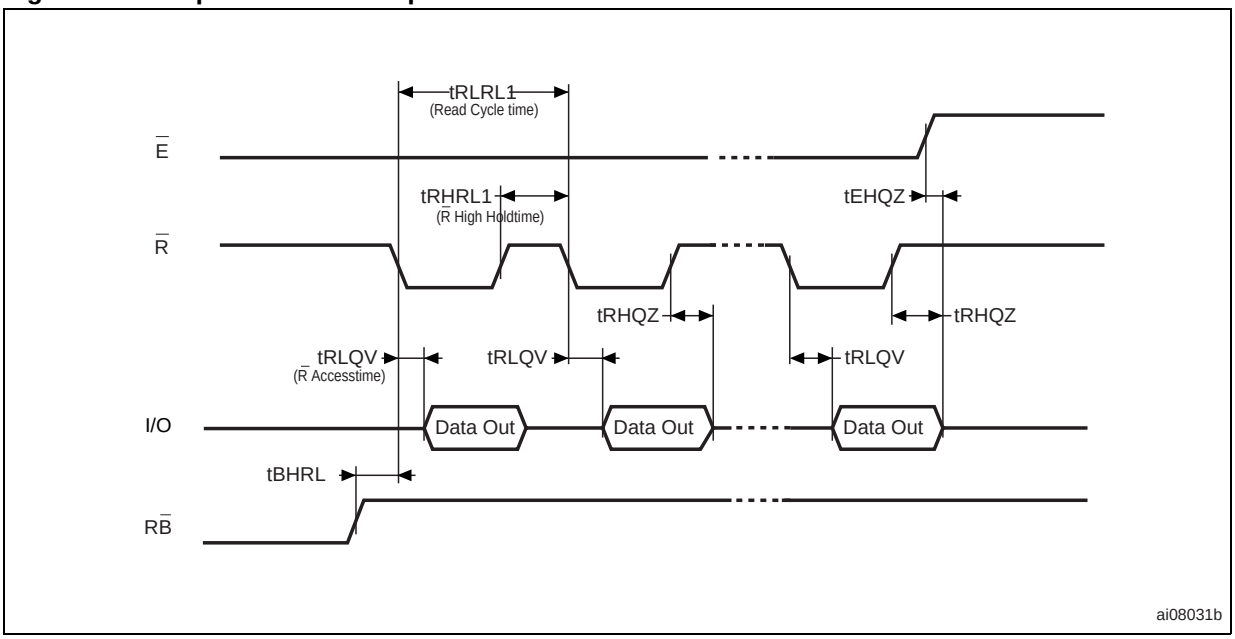


Figure 23. Data Input Latch AC Waveforms



1. Data In Last is 2112.

Figure 24. Sequential Data Output after Read AC Waveforms



1. CL = Low, AL = Low, W = High.

Figure 25. Read Status Register AC Waveform

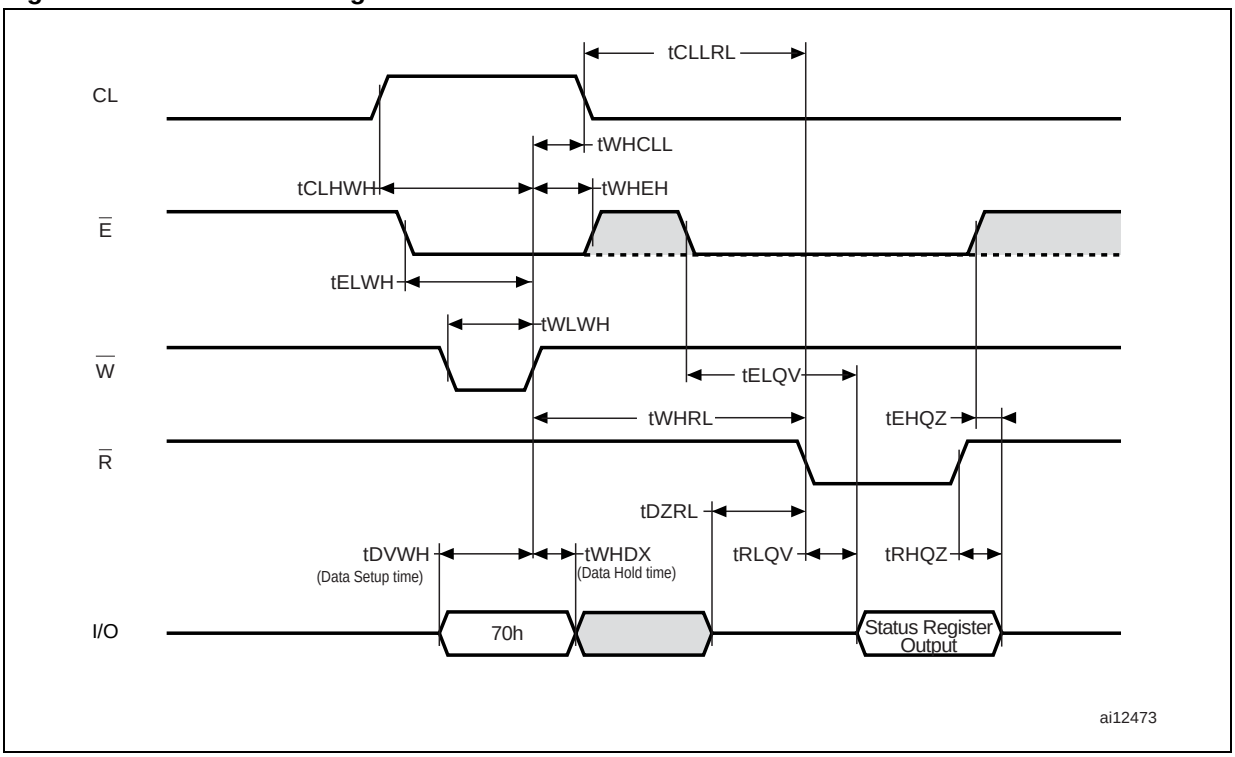
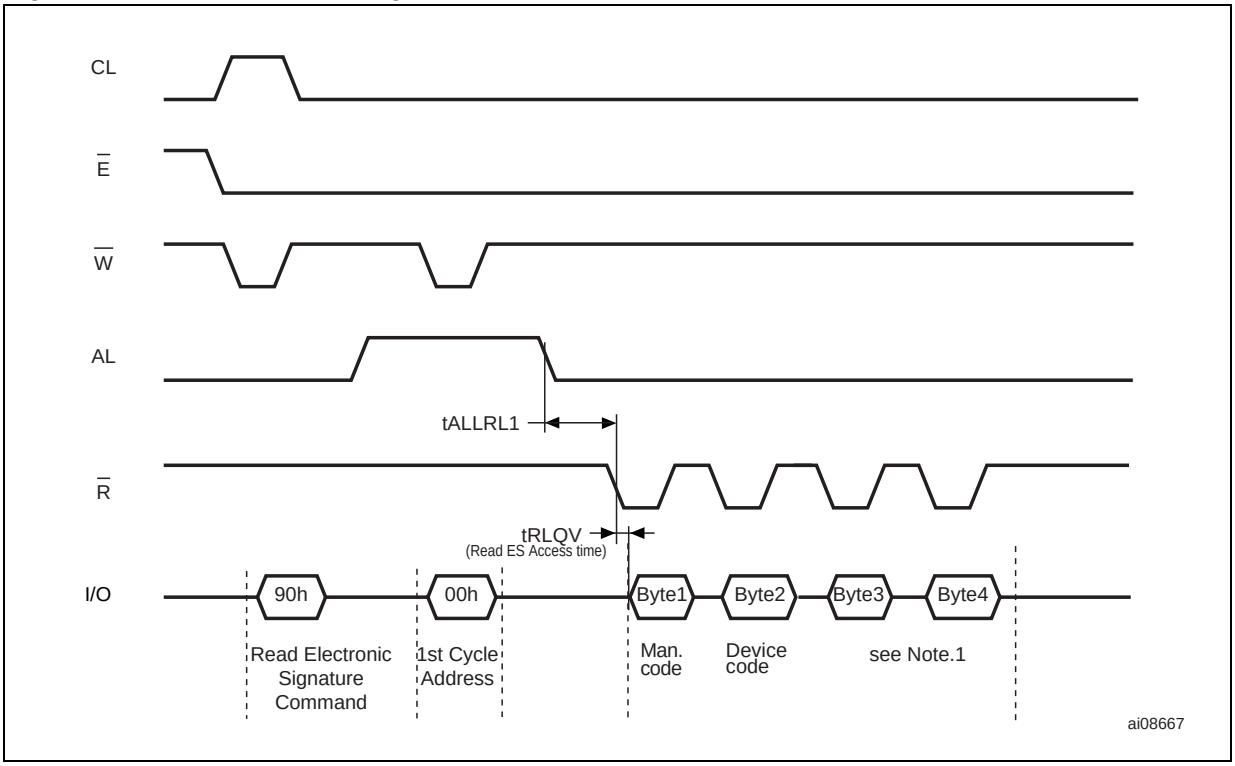


Figure 26. Read Electronic Signature AC Waveform



1. Refer to *Table 10* for the values of the Manufacturer and Device Codes, and to *Table 11* and *Table 12* for the information contained in Byte 3 and Byte 4.

Figure 27. Page Read Operation AC Waveform

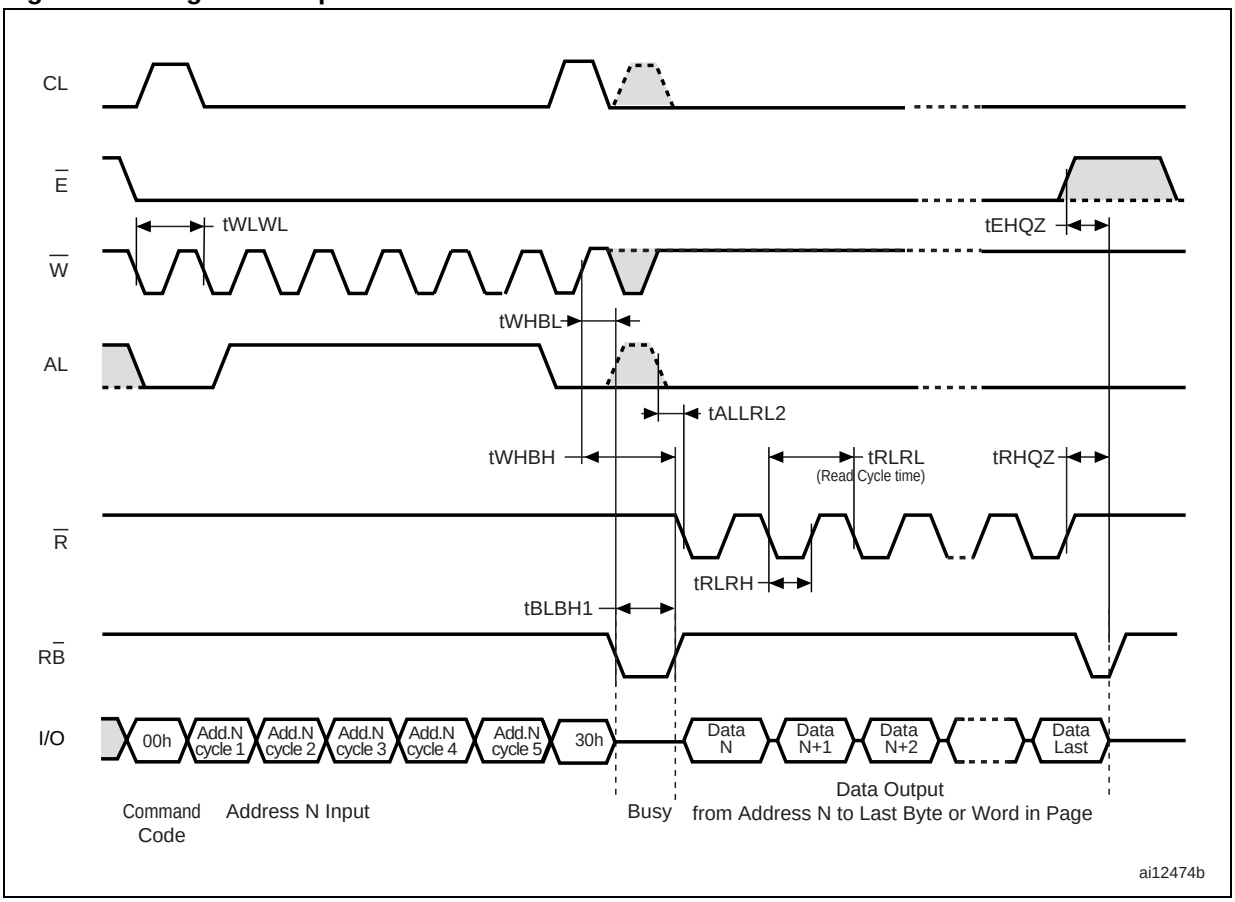


Figure 28. Page Program AC Waveform

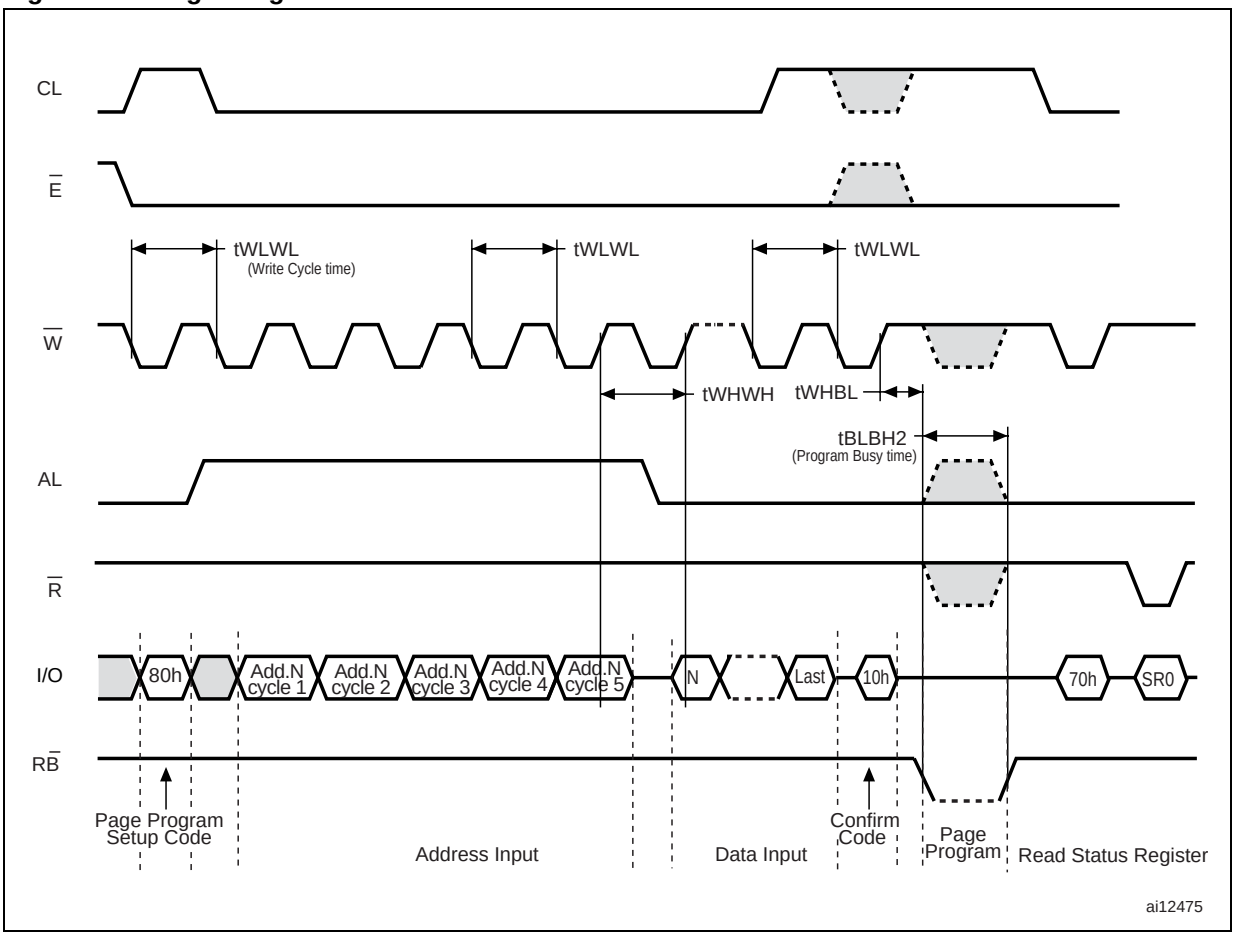


Figure 29. Block Erase AC Waveform

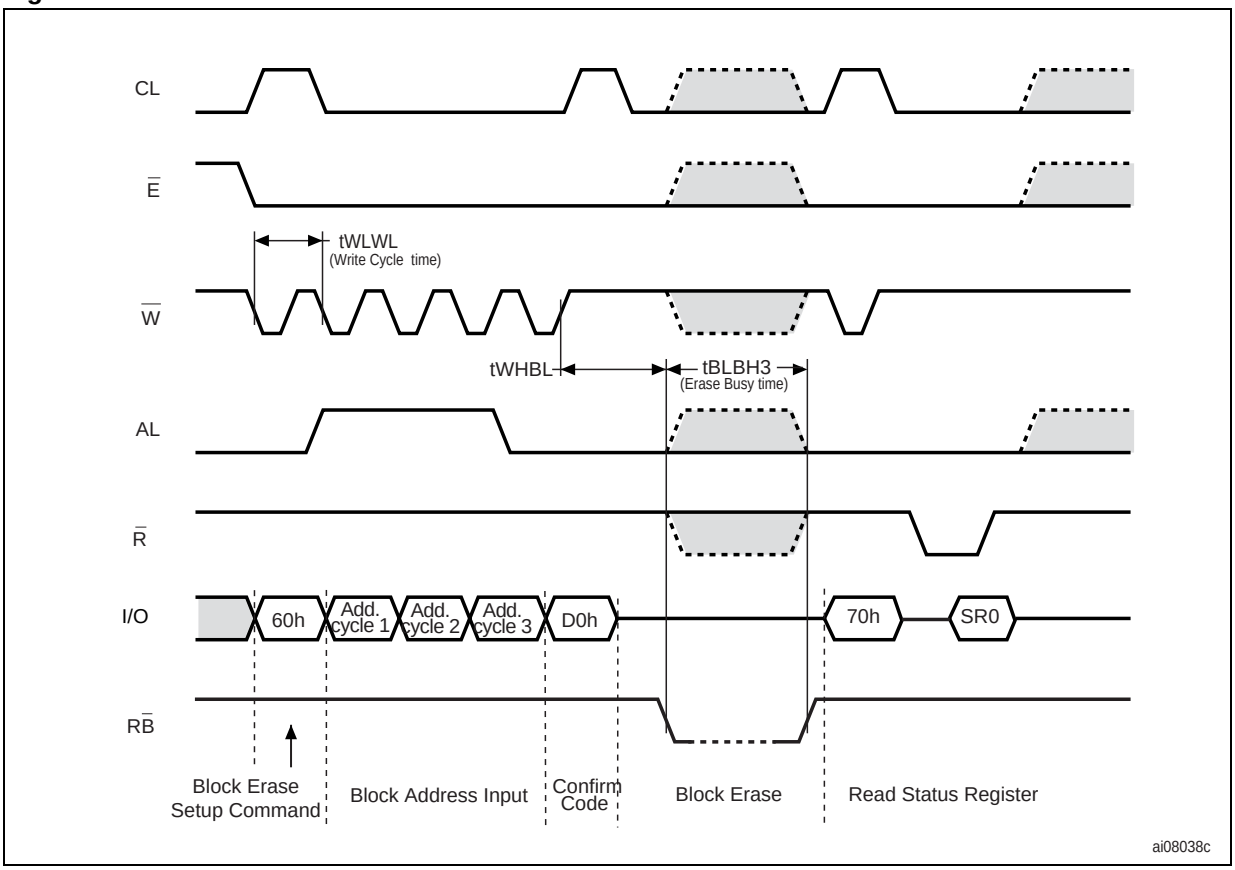


Figure 30. Reset AC Waveform

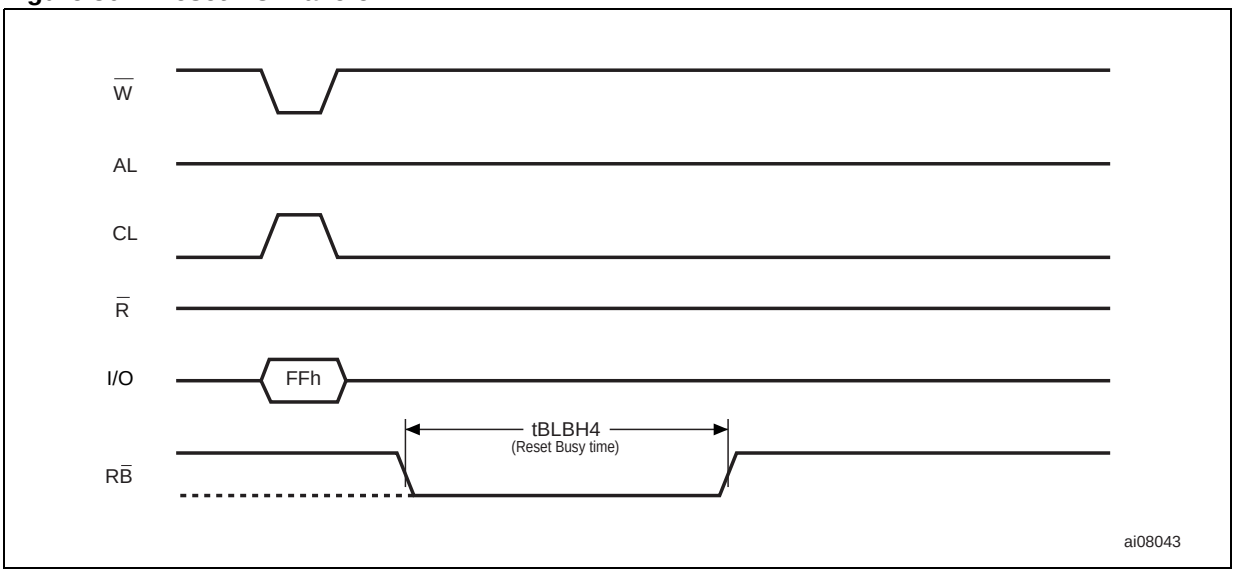


Figure 31. Program/Erase Enable Waveform

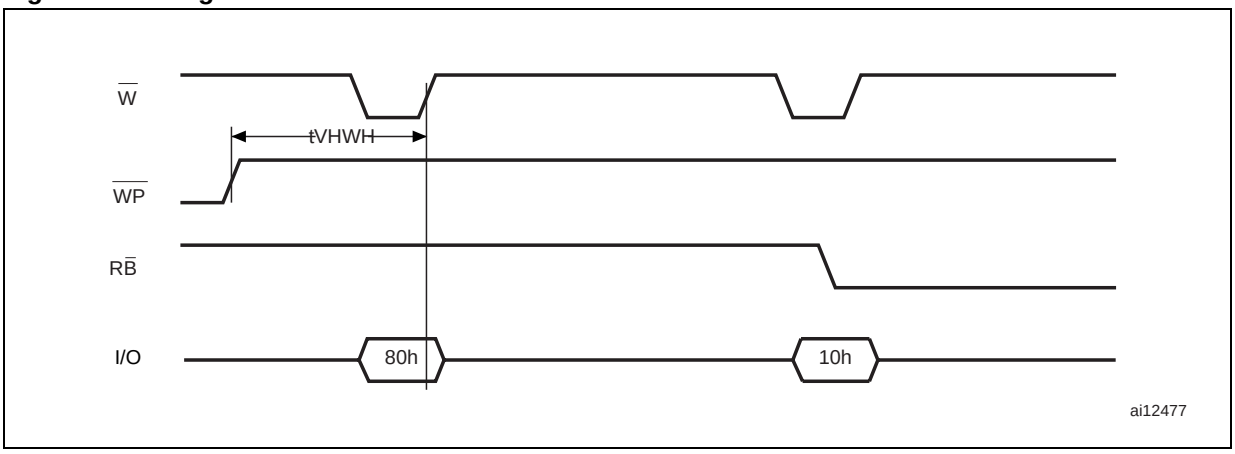
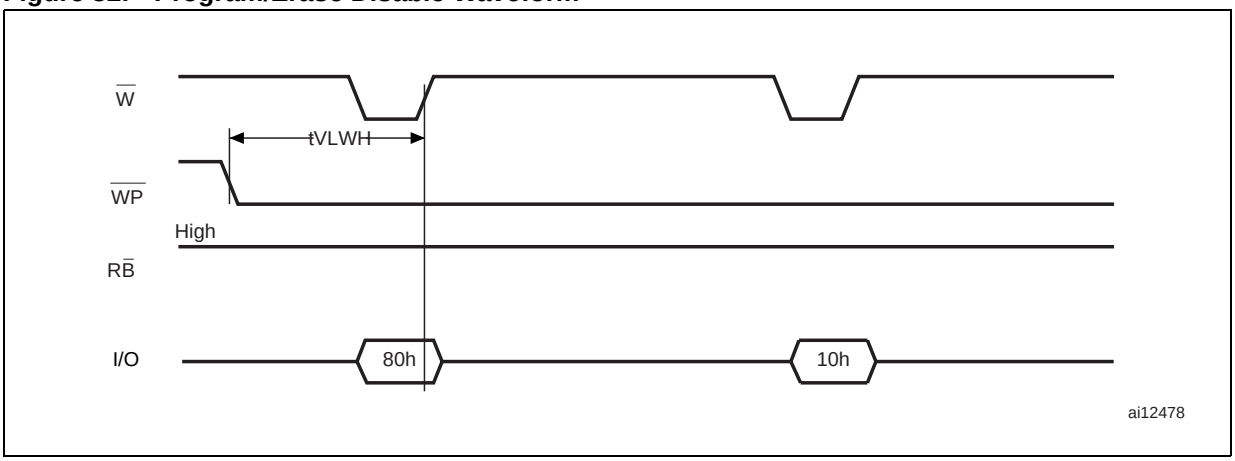


Figure 32. Program/Erase Disable Waveform



11.1 Ready/Busy Signal Electrical Characteristics

Figure 34, *Figure 33* and *Figure 35* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min(1.8V) = \frac{1.85V}{3mA + I_L}$$

$$R_P min(3V) = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 33. Ready/Busy AC Waveform

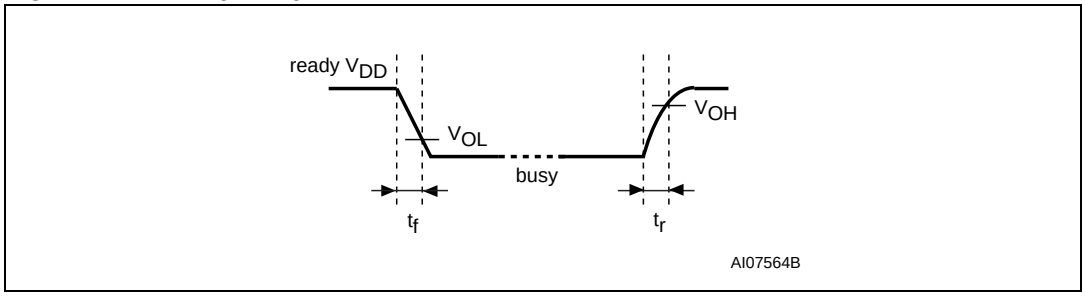


Figure 34. Ready/Busy Load Circuit

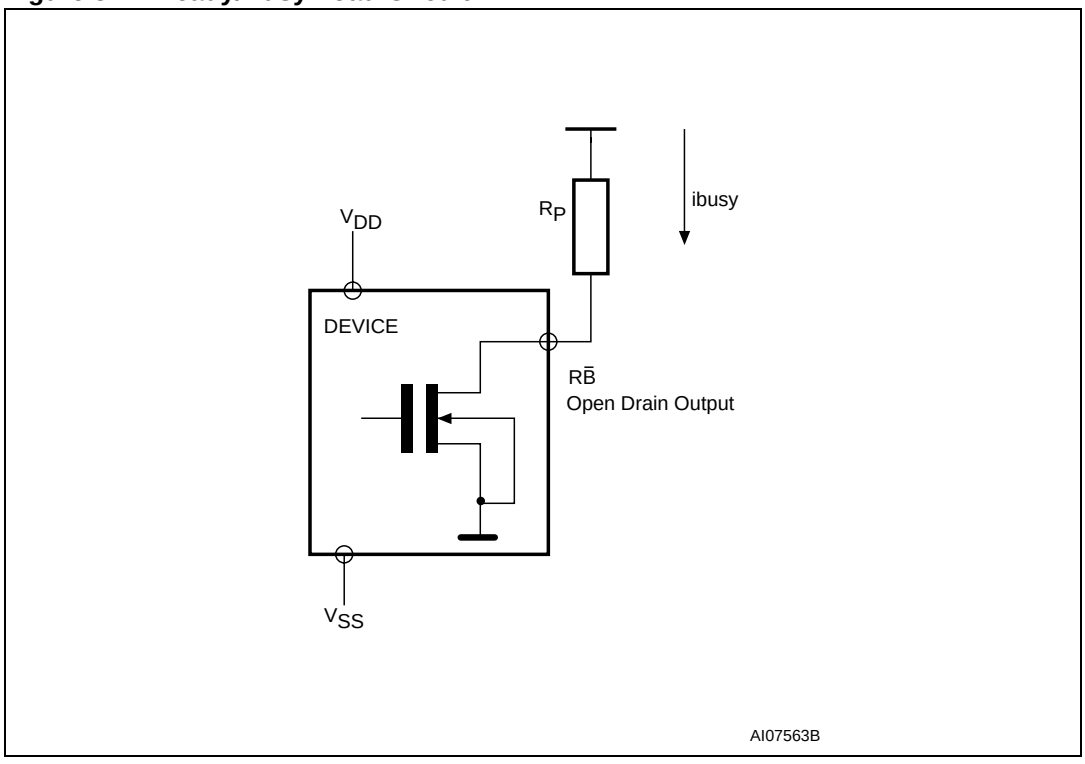
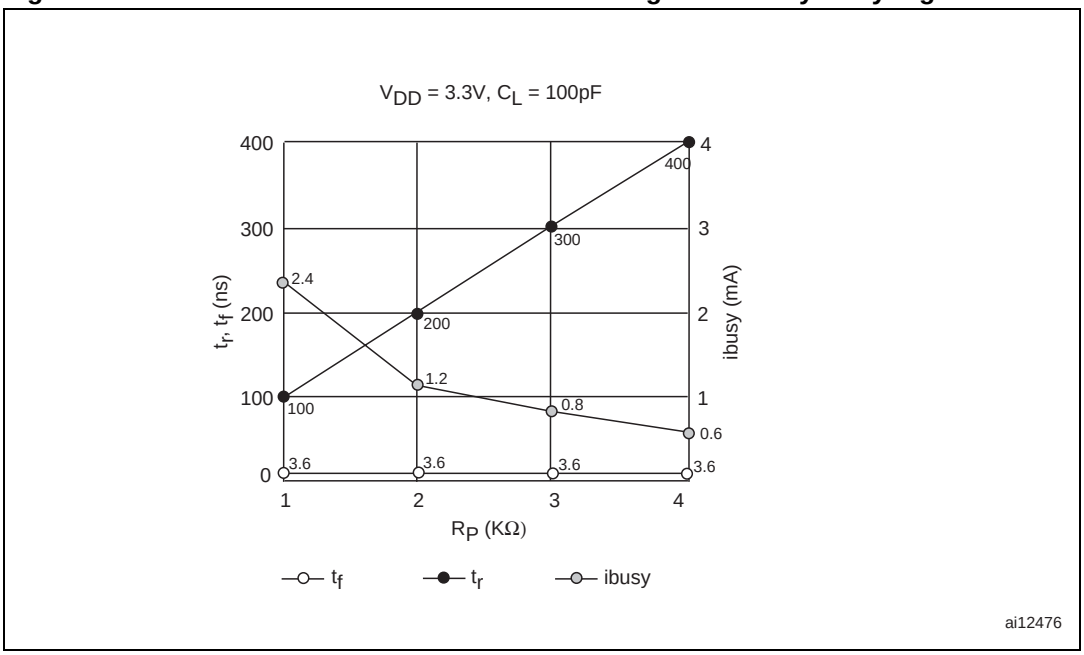


Figure 35. Resistor Value Versus Waveform Timings For Ready/Busy Signal



1. T = 25°C.

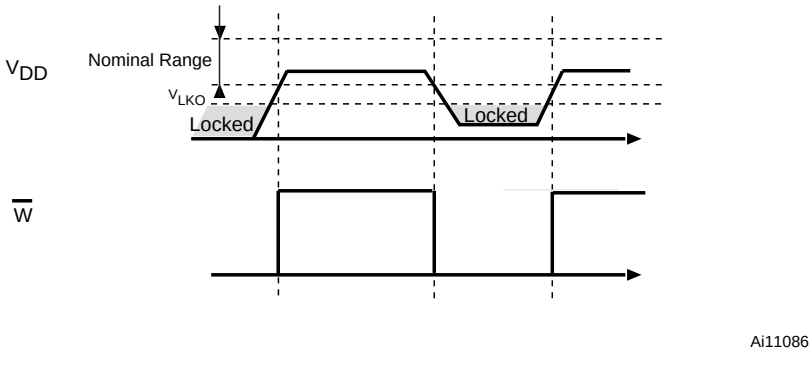
11.2 Data Protection

The ST NAND device is designed to guarantee Data Protection during Power Transitions.

A V_{DD} detection circuit disables all NAND operations, if V_{DD} is below the V_{LKO} threshold.

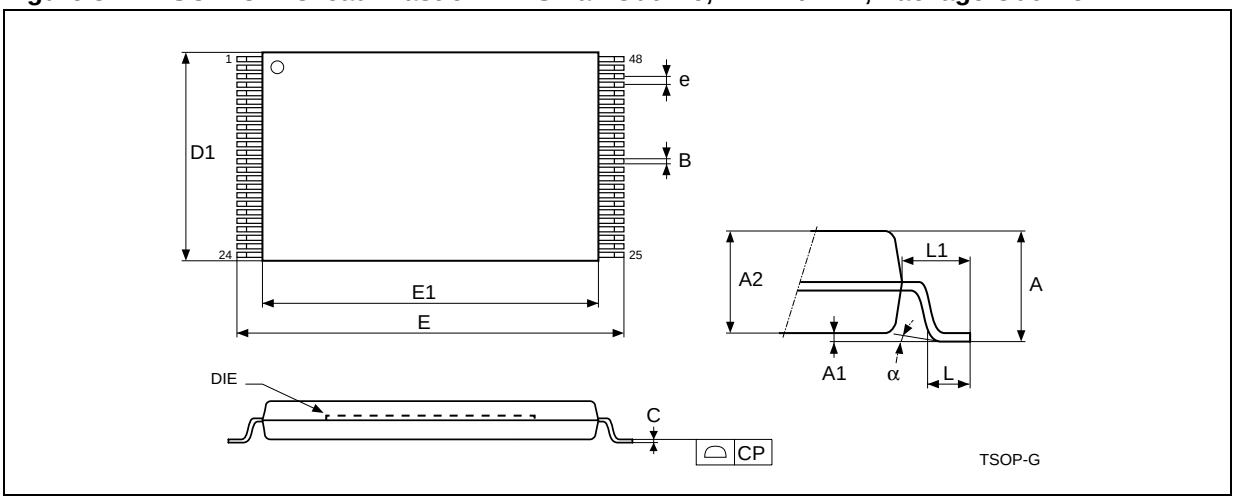
In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept low (V_{IL}) to guarantee hardware protection during power transitions as shown in the below figure.

Figure 36. Data Protection



12 Package mechanical

Figure 37. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Outline



1. Drawing is not to scale.

Table 22. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.080			0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
a	3°	0°	5°	3°	0°	5°

13 Part numbering

Table 23. Ordering Information Scheme

Example: NAND04GW3B2B N 6 E

Device Type

NAND Flash Memory

Density

04G = 4Gb

08G = 8Gb

Operating Voltage

W = V_{DD} = 2.7 to 3.6V

Bus Width

3 = x8

Family Identifier

B = 2112 Byte Page

Device Options

2 = Chip Enable Don't Care Enabled

Product Version

A = First Version (NAND08GW3B2A)

B= Second Version (NAND04GW3B2B)

Package

N = TSOP48 12 x 20mm (all devices)

Temperature Range

1 = 0 to 70 °C

6 = –40 to 85 °C

Option

E = Lead Free Package, Standard Packing

F = Lead Free Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits, in valid blocks, erased to ’1’. For further information on any aspect of this device, please contact your nearest ST Sales Office.

14 Revision history

Table 24. Document revision history

Date	Revision	Changes
14-Feb-2006	1.0	Initial release.
30-May-2006	2	NAND08GW3B2A added, and *Table 1: Product Description*, *Table 3: Valid Blocks*, *Table 5: Address Insertion*, *Table 6: Address Definition*, *Table 9: Status Register Bits* and *Table 23: Ordering Information Scheme* updated. t_{BLBH4} timing added in *Figure 7: Cache Read Operation*. *Table 8: Copy Back Program addresses* added in *Section 6.4: Copy Back Program*. Definition of Status Register bit SR6 updated in *Table 8: Copy Back Program addresses*. t_{WC}, t_{WP} minimum values updated in *Table 20: AC Characteristics for Command, Address, Data Input*. t_{EHEL}, t_{EHBL}, t_{RHBL} removed from *Figure 27: Page Read Operation AC Waveform* .

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